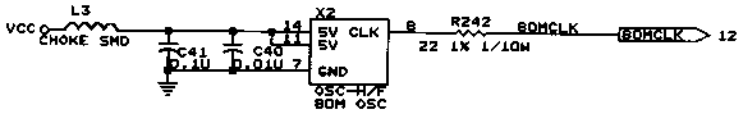
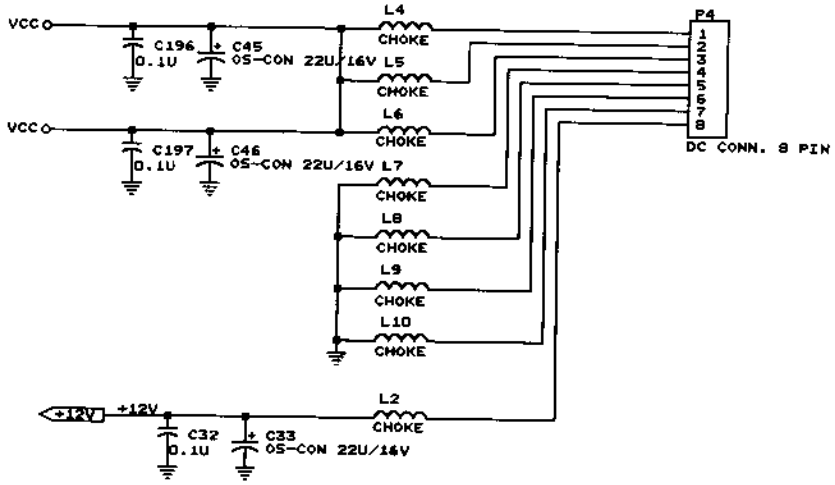
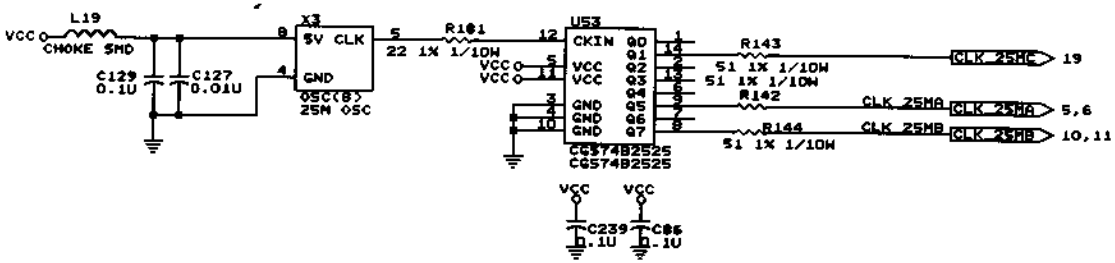


PLACED AS CLOSE AS POSSIBLE TO GT-48001A

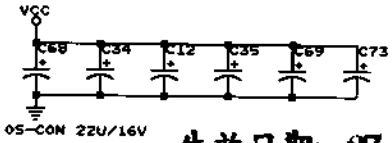
80 MHz FOR GT-48001A



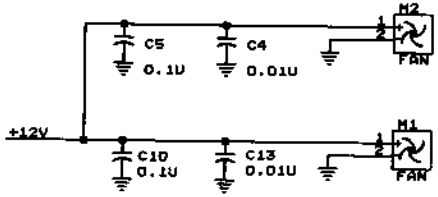


LAYOUT TRACES TO 4 LXT970
SHOULD BE AS SHORT AS POSSIBLE

25MHz CLOCK FOR 4 LXT970

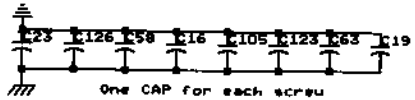


POWER CONNECTOR



Becareful of the placement of M1, M2
Don't put M1, M2 in front of the FANs

FAN CONNECTORS



LINK
1
2
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10
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12
13
14
15
16
17
18
19
20

生效日期: 87. 2. 26

15.2 X 11.7

D-Link Corp.

Approved	張福財	PREPARED BY: VINCENT WU	吳玉敏
Checked	張福財	ISSUE DATE : DEC 26, 1996	
DOC. NO.: 305DES2212---A1-	Version: A	Title: ES-2212BI : POWER/FAN CONN. & SYS CLOCK	
		Size: B Document Number: 2102 2202	REV: A1
		Date: July 21, 1997 Sheet 1 of 20	

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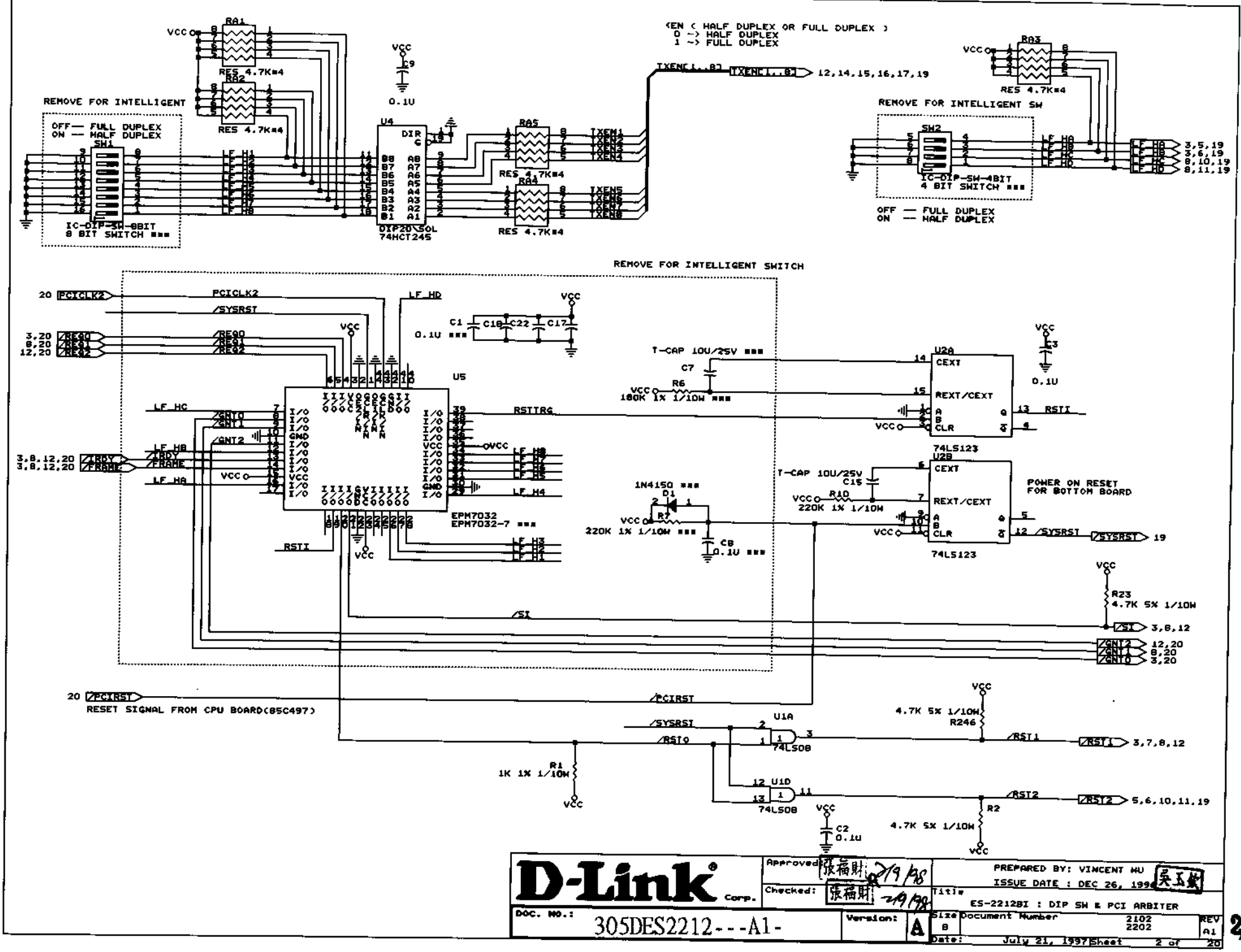
REMOVE FOR INTELLIGENT
OFF— FULL DUPLEX
ON — HALF DUPLEX
SW1
IC-DIP-SW-8BIT
8 BIT SWITCH ###
RA1
RES 4.7K*4
RA2
RES 4.7K*4
VCC
C9
0.1U
U4
DIR
OE
DIP20 SOL
74HCT245
RA5
RES 4.7K*4
RA4
RES 4.7K*4
TXEN (HALF DUPLEX OR FULL DUPLEX)
0 -> HALF DUPLEX
1 -> FULL DUPLEX
TXEN[1..8]
TXEN[1..8] 12,14,15,16,17,19
RA3
RES 4.7K*4
REMOVE FOR INTELLIGENT SW
SW2
IC-DIP-SW-4BIT
4 BIT SWITCH ###
OFF — FULL DUPLEX
ON — HALF DUPLEX
3,5,19
3,6,19
8,10,19
8,11,19
REMOVE FOR INTELLIGENT SWITCH
20 PCICLK2
PCICLK2
/SYSRST
LF_HD
C1
C18
C22
C17
0.1U ###
3,20 /REQ0
8,20 /REQ1
12,20 /REQ2
/REQ0
/REQ1
/REQ2
U5
LF_HC
/GNT0
/GNT1
/GNT2
LF_HB
3,8,12,20 /RDY
3,8,12,20 /FRAME
LF_HA
RSTIRQ
LF_H8
LF_H4
LF_H3
EPM7032
EPM7032-7 ###
RSTI
1N4150 ###
D1
R7
220K 1% 1/10W ###
C8
0.1U ###
T-CAP 10U/25V ###
C7
R6
180K 1% 1/10W ###
U2A
CEXT
REXT/CEXT
A
B
CLR
Q
13 RSTI
C3
0.1U
74LS123
U2B
T-CAP 10U/25V
C15
R10
220K 1% 1/10W
POWER ON RESET
FOR BOTTOM BOARD
12 /SYSRSI
/SYSRST 19
R23
4.7K 5% 1/10W
/SI 3,8,12
/GNT2 12,20
/GNT1 8,20
/GNT0 3,20
20 /PCIRST
RESET SIGNAL FROM CPU BOARD(85C497)
/PCIRST
U1A
/SYSRSI
/RSI0
74LS08
R1
1K 1% 1/10W
4.7K 5% 1/10W
R246
/RSI1
/RST1 3,7,8,12
U1D
/RSI2
/RST2 5,6,10,11,19
R2
4.7K 5% 1/10W
C2
0.1u
D-Link Corp.
Approved: 張福財 2/9/98
Checked: 張福財 2/9/98
PREPARED BY: VINCENT WU
ISSUE DATE : DEC 26, 1996
吳玉敏
Title
ES-2212BI : DIP SW & PCI ARBITER
DOC. NO.: 305DES2212---A1-
Version: A
Size B
Document Number 2102 2202
REV A1
Date: July 21, 1997 Sheet 2 of 20

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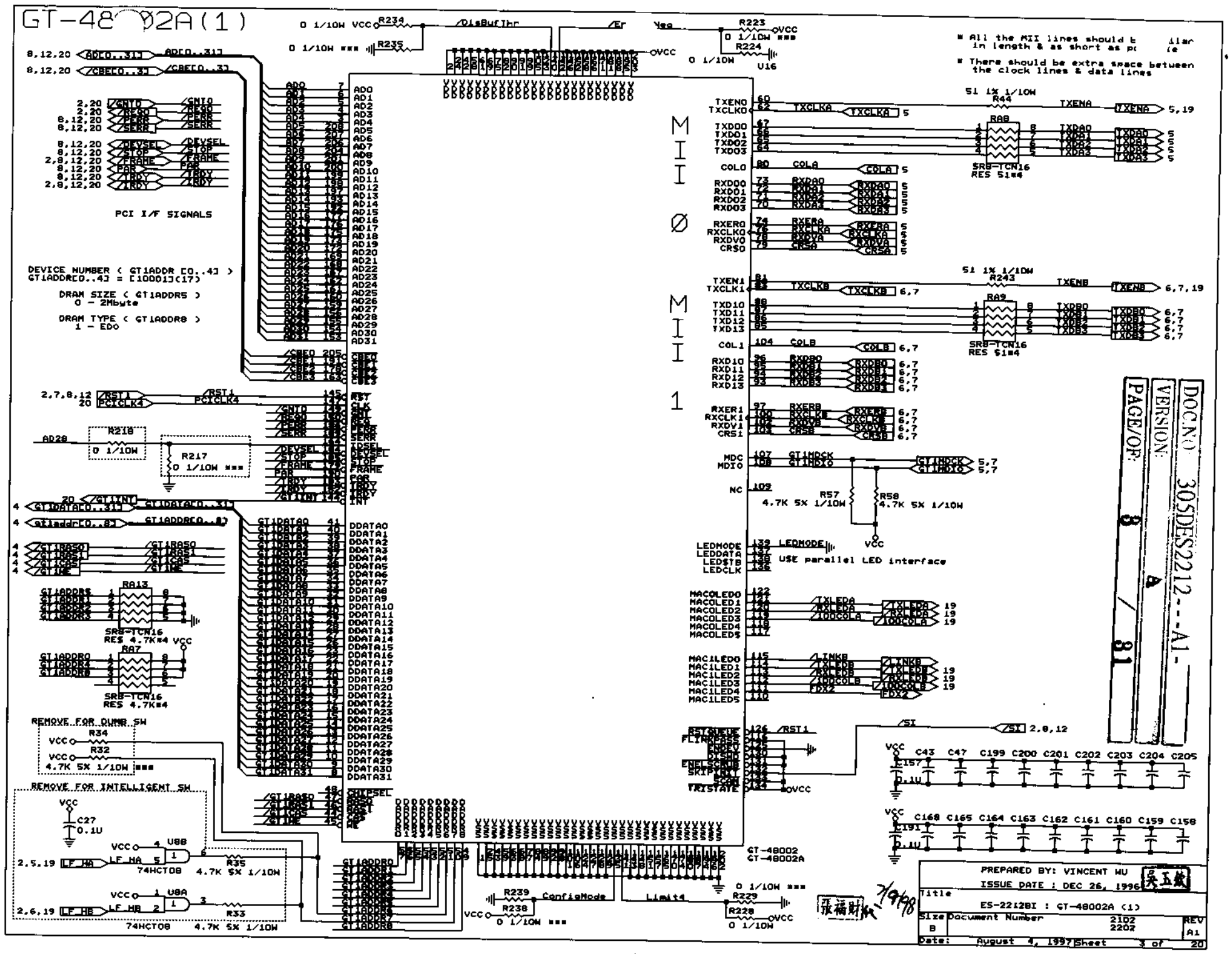
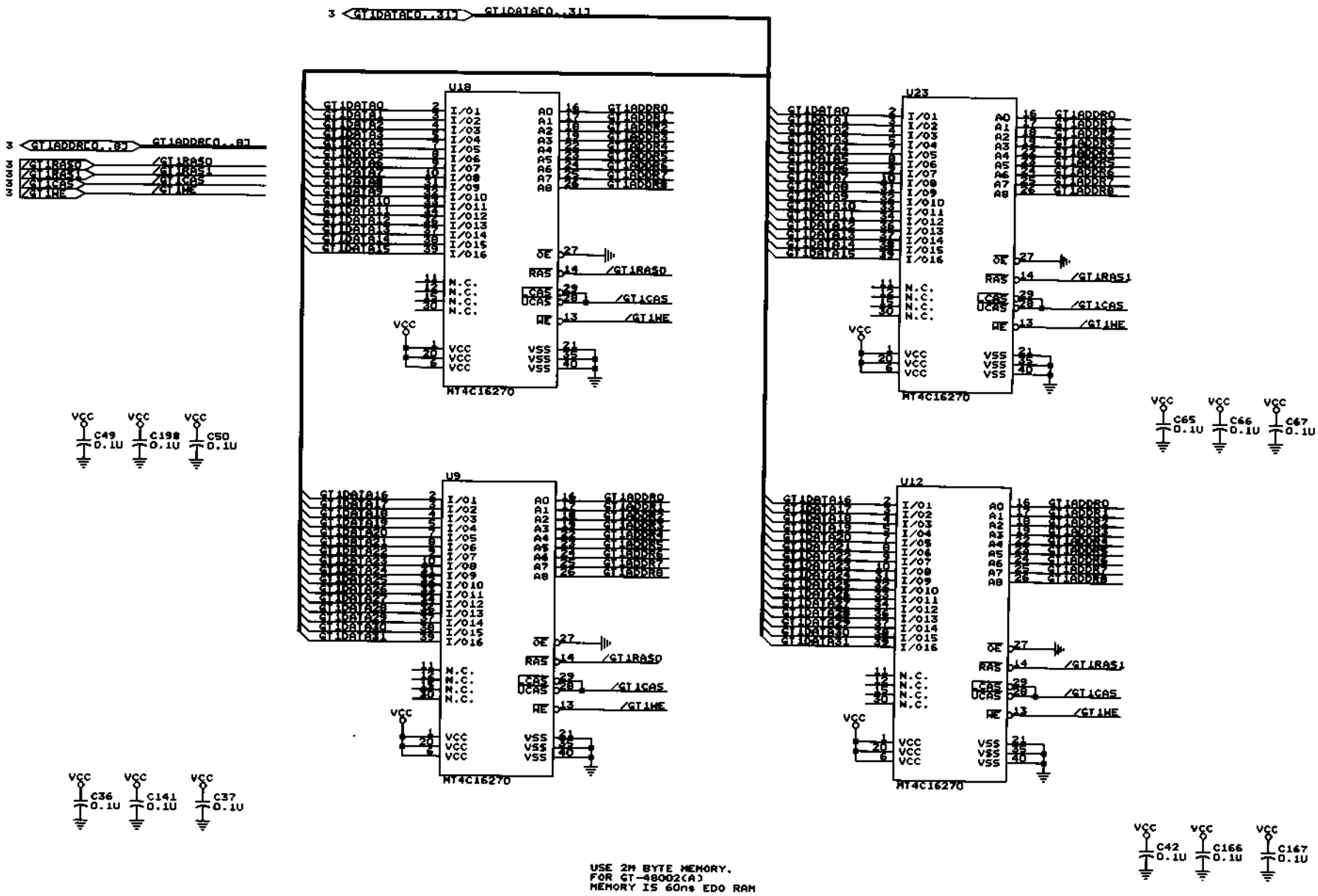

GT-48002A(1)
* All the MII lines should b ilar in length & as short as p le
* There should be extra space between the clock lines & data lines
PCI I/F SIGNALS
DEVICE NUMBER (GT1ADDR [0..4])
GT1ADDR[0..4] = [10001](17)
DRAM SIZE (GT1ADDR5)
0 - 2Mbyte
DRAM TYPE (GT1ADDR8)
1 - EDO
MII Ø
MII 1
USE parallel LED interface
REMOVE FOR DUMB SW
REMOVE FOR INTELLIGENT SW
74HCT08
GT-48002
GT-48002A
ConfigMode
Limit4
DOC.NO: 305DES2212---A1-
VERSION: A
PAGE/OF: 8 / 81
PREPARED BY: VINCENT WU
ISSUE DATE : DEC 26, 1996
Title
ES-2212BI : GT-48002A (1)
Size B
Document Number 2102 2202
REV A1
Date: August 4, 1997
Sheet 3 of 20

FOR GT-48002A(1)



USE 2M BYTE MEMORY.
FOR GT-48002(A)
MEMORY IS 60ns EDO RAM

D-Link® Corp.	Approved: 張福財 2/9/98	PREPARED BY: VINCENT WU 吳玉欽	
	Checked: 張福財 2/9/98	ISSUE DATE : DEC 26, 1996	
		Title: ES-2212BI : DRAM FOR GT-48002A (1)	
DOC. NO.: 305DES2212---A1-	Version: A	Size: B	Document Number: 2102 2202 REV: A1
		Date: July 16, 1997	Sheet 4 of 20

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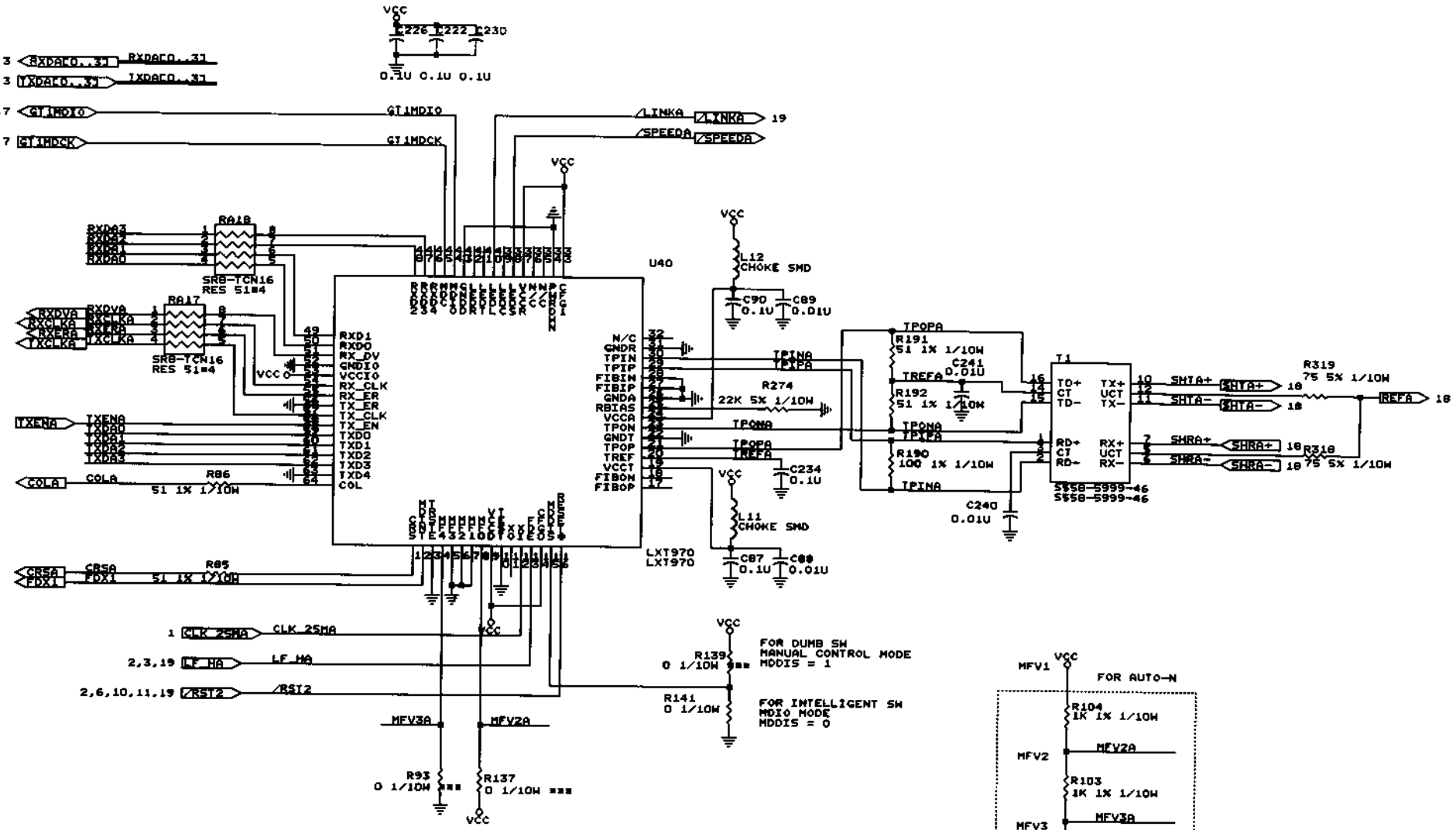


*MANUAL CONTROL MODE SETTING

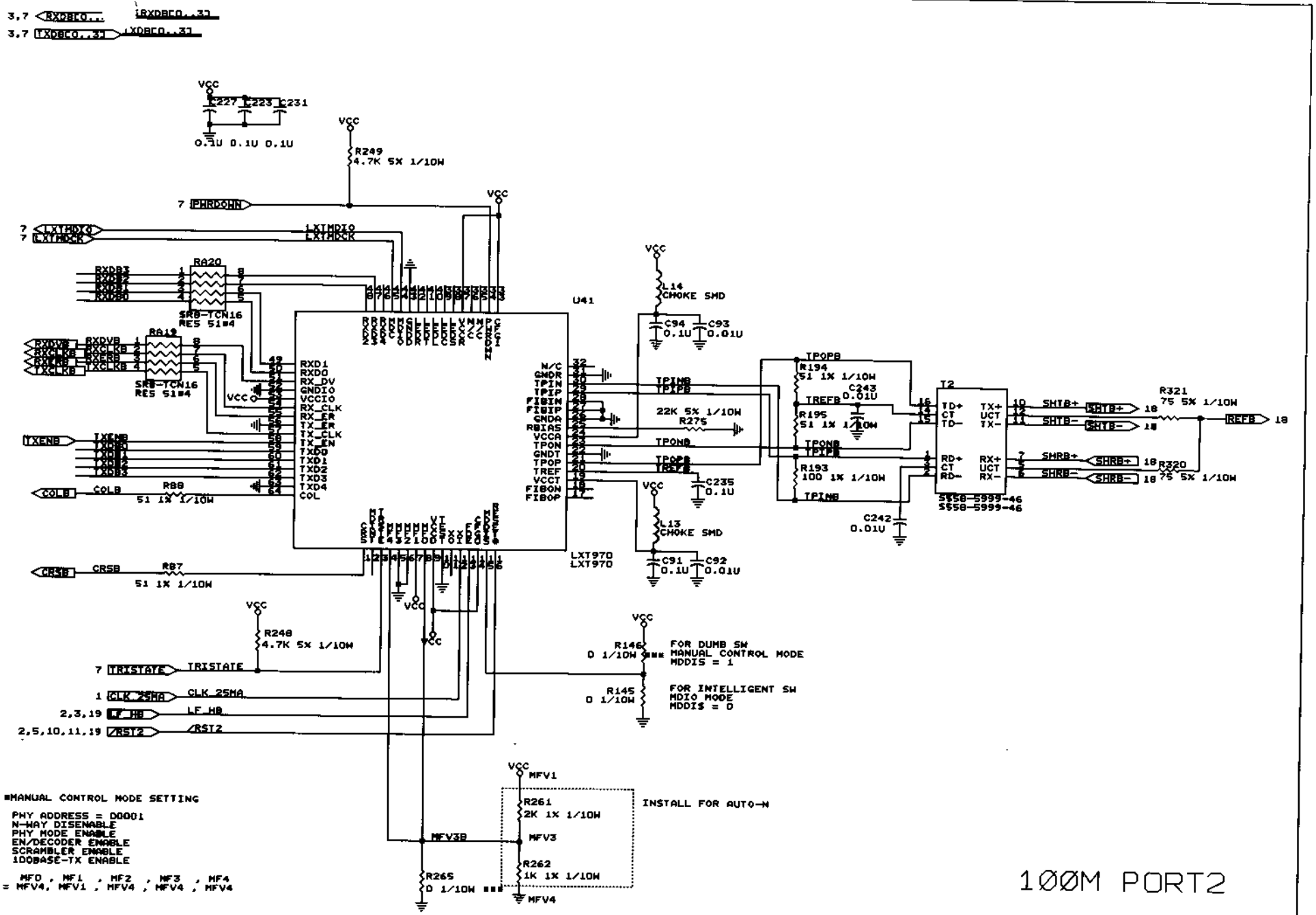
PHY ADDRESS = 00001
N-WAY DISENABLE
PHY MODE ENABLE
EN/DECODER ENABLE
SCRAMBLER ENABLE
100BASE-TX ENABLE

MF0 , MF1 , MF2 , MF3 , MF4
= MFV1, MFV4 , MFV4 , MFV4 , MFV4

CFGIO..13 = 11 (100M, DISABLE 10BASE-T LINK TEST)

10ØM PORT1

D-Link Corp.	Approved 張福財	PREPARED BY: VINCENT WU	吳玉敏
	Checked 張福財	ISSUE DATE : DEC 26, 1996	
DOC. NO.: 305DES2212---A1-	Version: A	Title: ES-2212BI : 100M PORT1 CKT	
		Size: A Document Number: 3102 2202	REV: A1
		Date: August 4, 1997 Sheet 5 of 20	



*MANUAL CONTROL MODE SETTING

PHY ADDRESS = D0001
N-WAY DISENABLE
PHY MODE ENABLE
EN/DECODER ENABLE
SCRAMBLER ENABLE
100BASE-TX ENABLE

MF0 , MF1 , MF2 , MF3 , MF4
= MFV4, MFV1 , MFV4 , MFV4 , MFV4

CFG[0..1] = 11 (100M, DISABLE 10BASE-T LINK TEST)

100M PORT2

D-Link Corp.	Approved: 張福財 2/9/98	PREPARED BY: VINCENT WU ISSUE DATE : DEC 26, 1996 吳玉欽	
	Checked: 張福財 2/9/98	Title: ES-2212BI : 100M PORT2 CKT	
DOC. NO.: 305DES2212---A1-	Version: A	Size: B Document Number: 2102 2202	REV: A1
		Date: August 4, 1997 Sheet 6 of 20	

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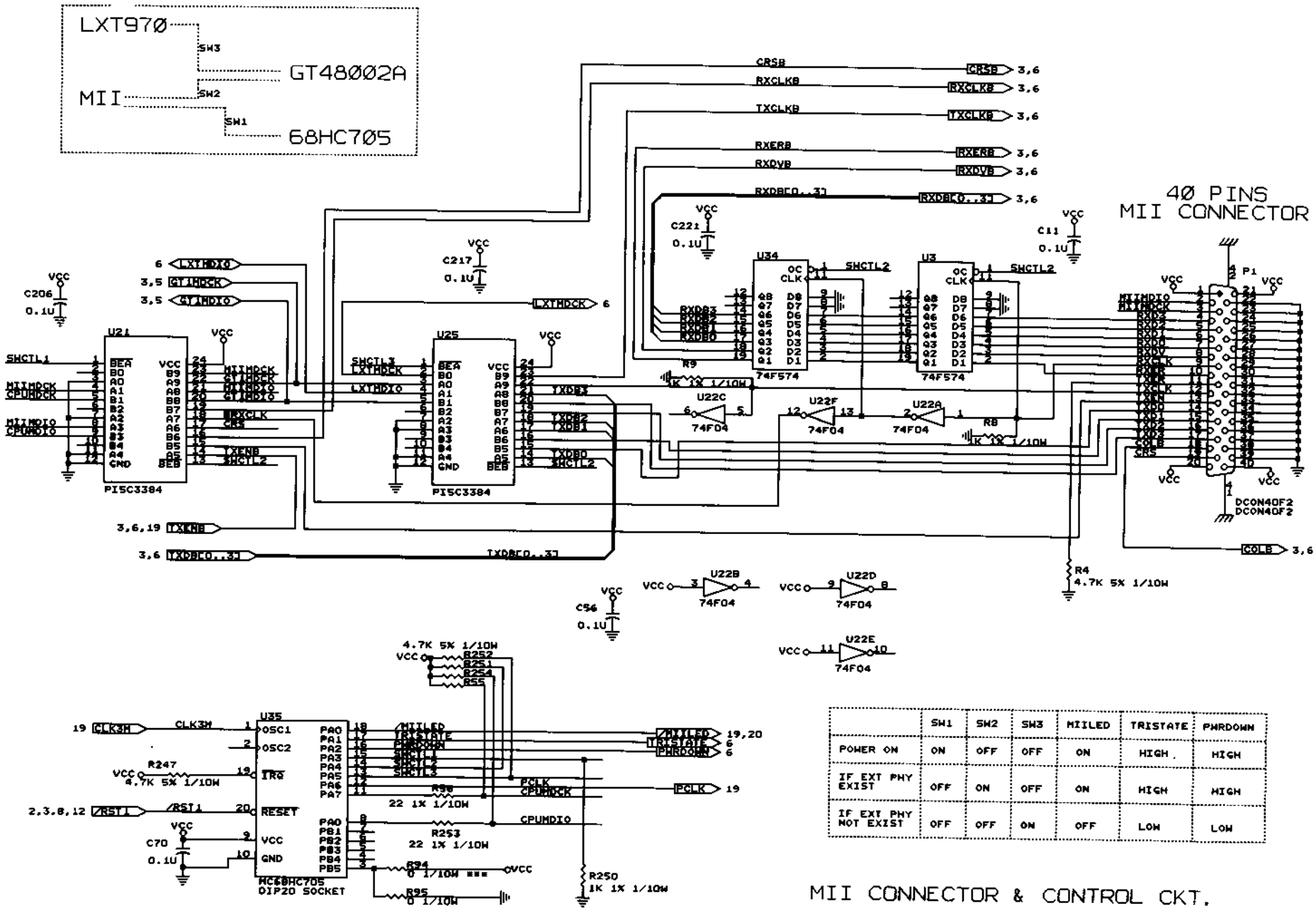

	SW1	SW2	SW3	MIILED	TRISTATE	PWRDOWN
POWER ON	ON	OFF	OFF	ON	HIGH	HIGH
IF EXT PHY EXIST	OFF	ON	OFF	ON	HIGH	HIGH
IF EXT PHY NOT EXIST	OFF	OFF	ON	OFF	LOW	LOW

MII CONNECTOR & CONTROL CKT.

FOR READING THE EXTERNAL PHY
MICRO-P FOR PROCESSING EXTERNAL 100M PHY

D-Link Corp.

Approved: 張福財 7/9/98	PREPARED BY: VINCENT WU 吳玉鐵	
Checked: 張福財 7/9/98	ISSUE DATE : DEC 26, 1996	
DOC. NO.: 305DES2212---A1-	Version: A	Title: ES-2212BI : 100M MII CONN. & CONTROL CKT
		Size: B Document Number: 2102 2202 REV A1
		Date: July 16, 1997 Sheet 7 of 20

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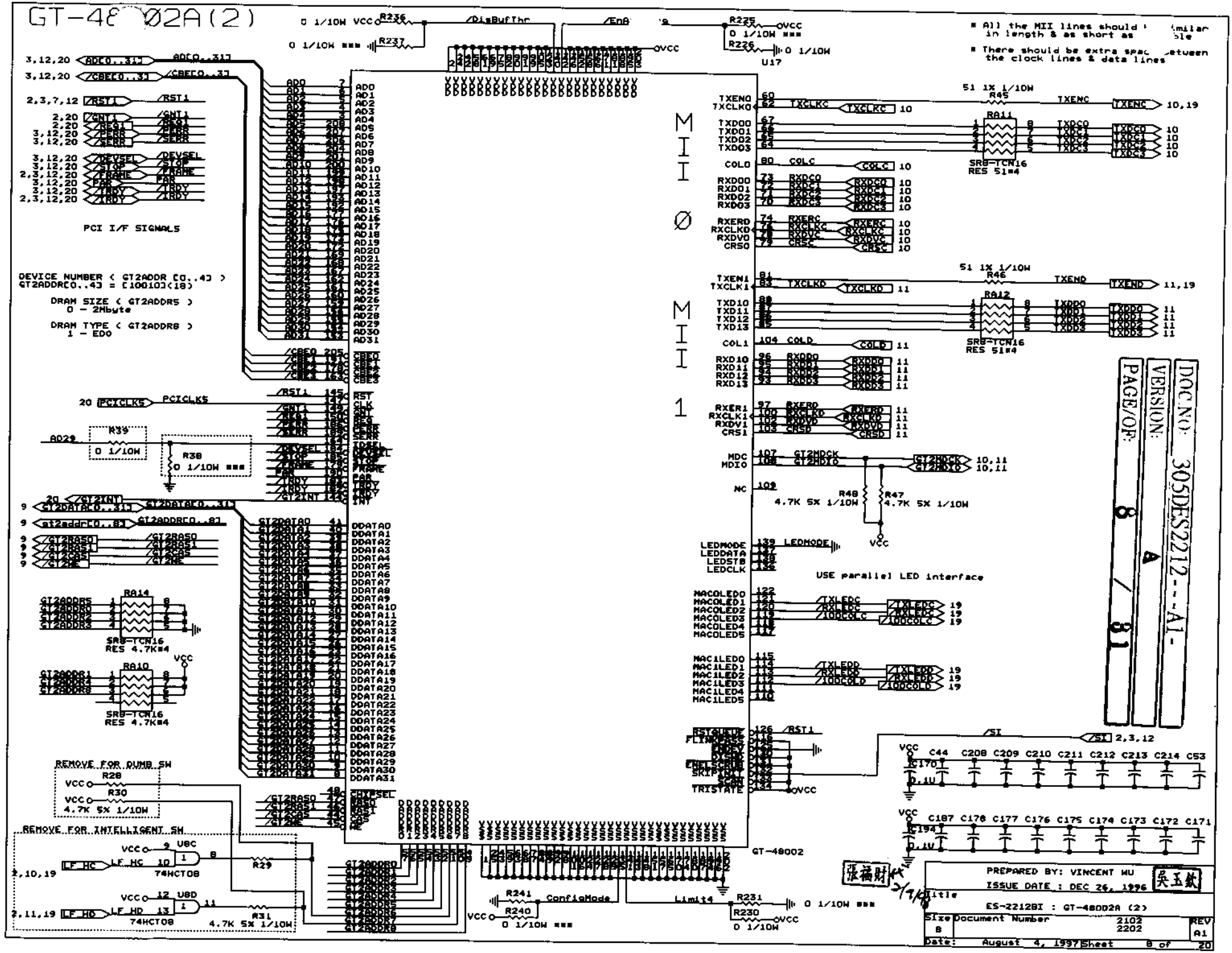
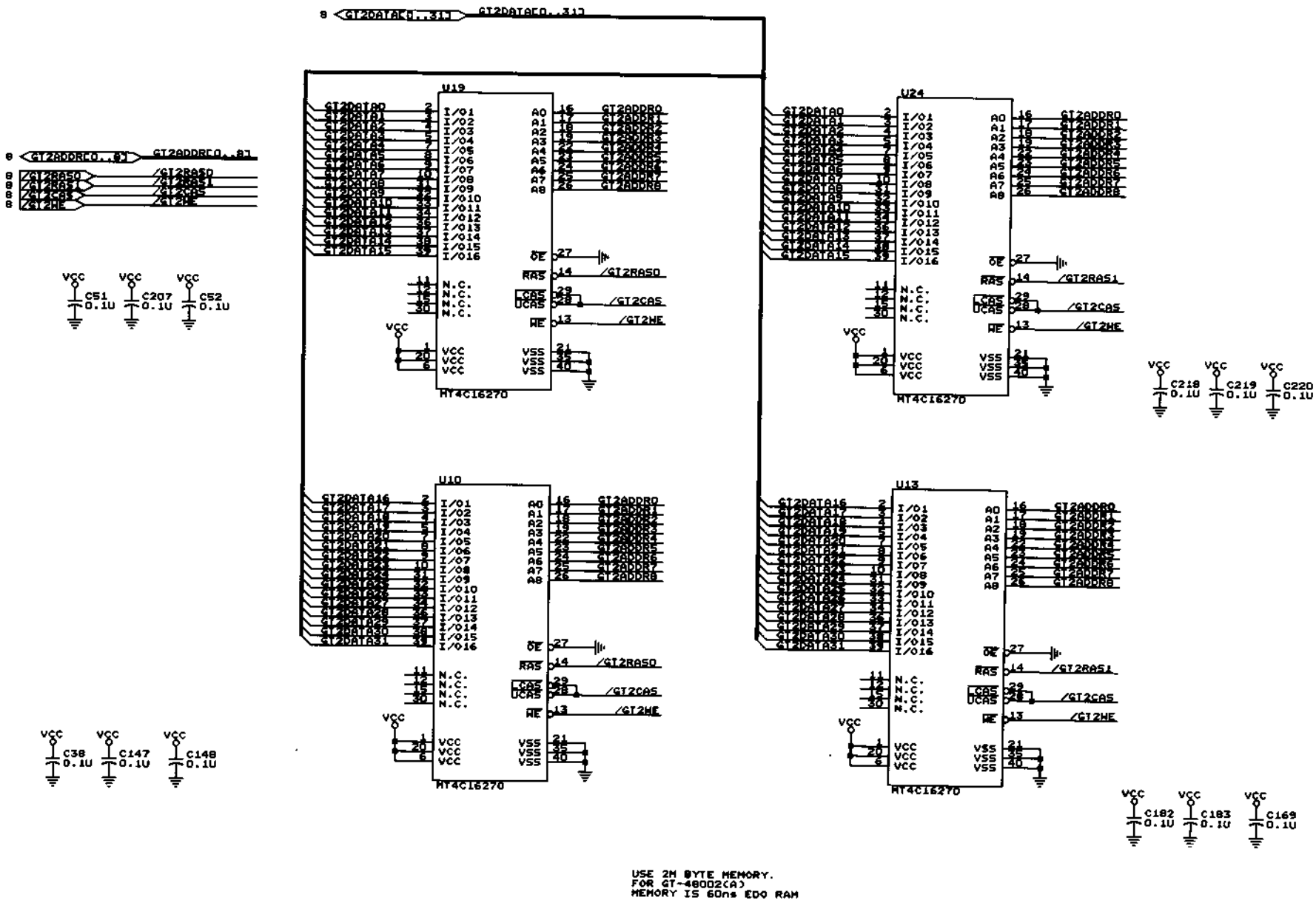

GT-48002A(2)
PCI I/F SIGNALS
DEVICE NUMBER (GT2ADDR [0..4]) = [10010](18)
DRAM SIZE (GT2ADDR5) 0 - 2Mbyte
DRAM TYPE (GT2ADDR8) 1 - EDO
REMOVE FOR DUMB SW
REMOVE FOR INTELLIGENT SW
MII0
MII1
USE parallel LED interface
GT-48002
PREPARED BY: VINCENT WU
ISSUE DATE : DEC 26, 1996
ES-2212BI : GT-48002A (2)
Document Number 2102 2202
REV A1
Date: August 4, 1997 Sheet 8 of 20
DOC.NO: 305DES2212--A1-
VERSION: A
PAGE/OF: 8 / 20

JR GT-48002A(2)



USE 2M BYTE MEMORY.
FOR GT-48002(A)
MEMORY IS 60ns EDO RAM

D-Link Corp.

Approved: 張福財 2/9/98
Checked: 張福財 2/9/98
PREPARED BY: VINCENT WU 吳玉鈸
ISSUE DATE : DEC 26, 1996

DOC. NO.: 305DES2212---A1-
Version: A
Title: ES-2212BI : DRAM FOR GT-48002A (2)
Size: B
Document Number: 2102 2202
REV: A1
Date: July 16, 1997 Sheet 9 of 20

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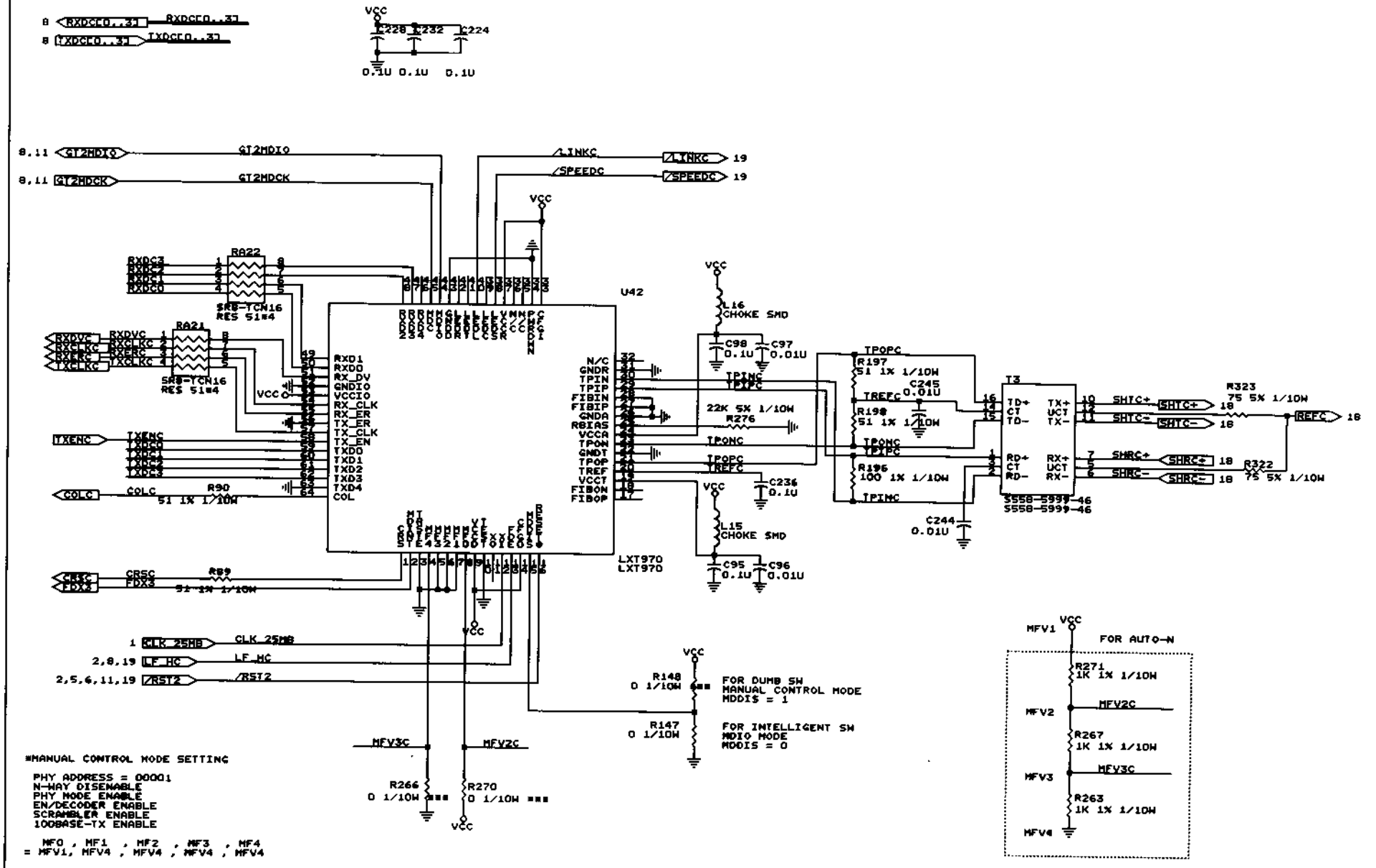

D-Link Corp.	Approved: 張福財	PREPARED BY: VINCENT WU 吳玉敏	
	Checked: 張福財	ISSUE DATE : DEC 26, 1996	
DOC. NO.: 305DES2212---A1-	Version: A	Title: ES-2212BI : 100M PORT3 CKT	
		Size: B Document Number: 2102 2202	REV: A1
		Date: August 4, 1997 Sheet 10 of 20	

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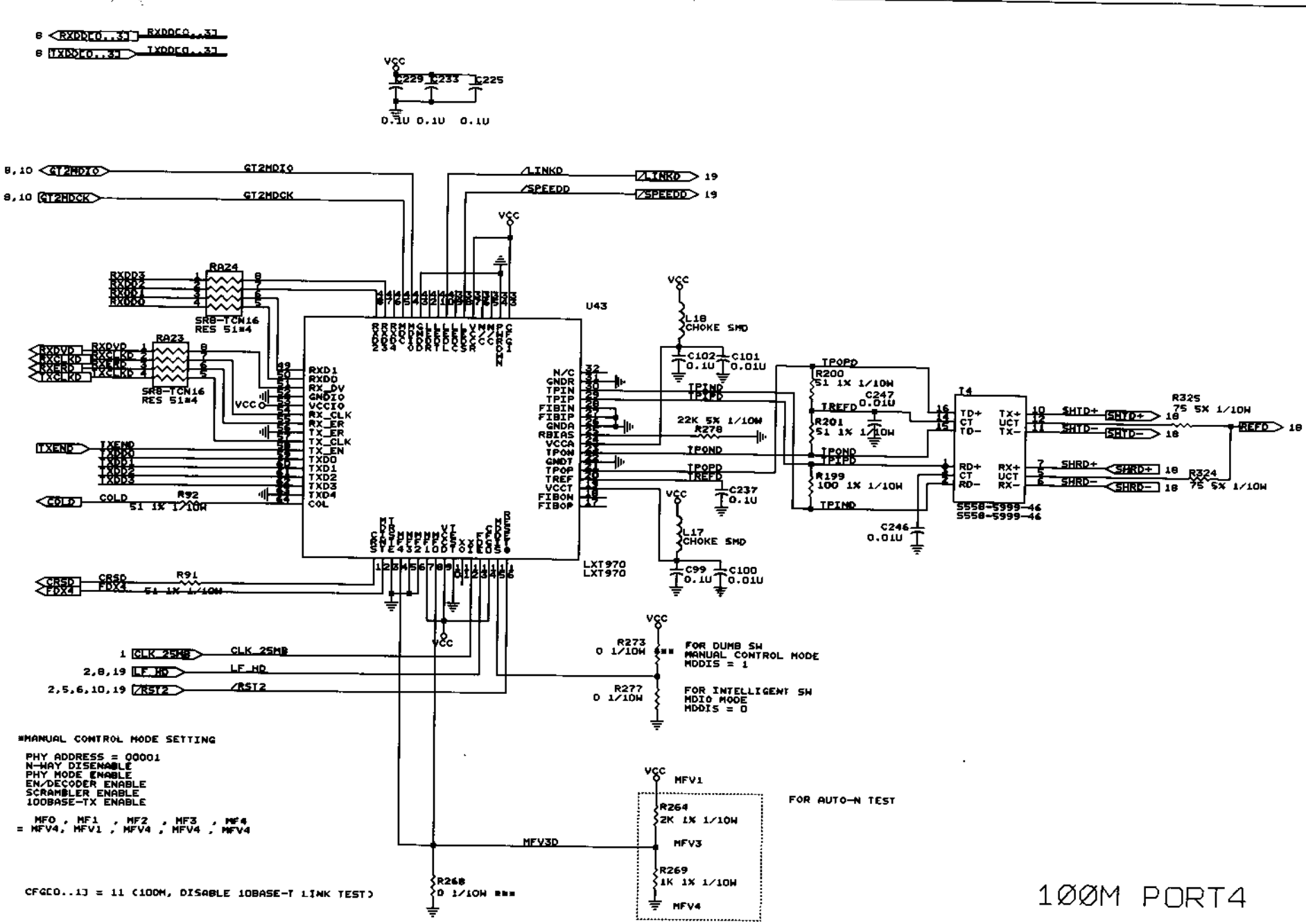

D-Link Corp.

Approved: 張福財	PREPARED BY: VINCENT WU	吳玉歆
Checked: 張福財	ISSUE DATE : DEC 26, 1996	
	Title: ES-2212BI : 100M PORT4 CKT	
DOC. NO.: 305DES2212---A1-	Version: A	Size: B; Document Number: 2102 2202; REV: A1
		Date: August 4, 1997; Sheet 11 of 20

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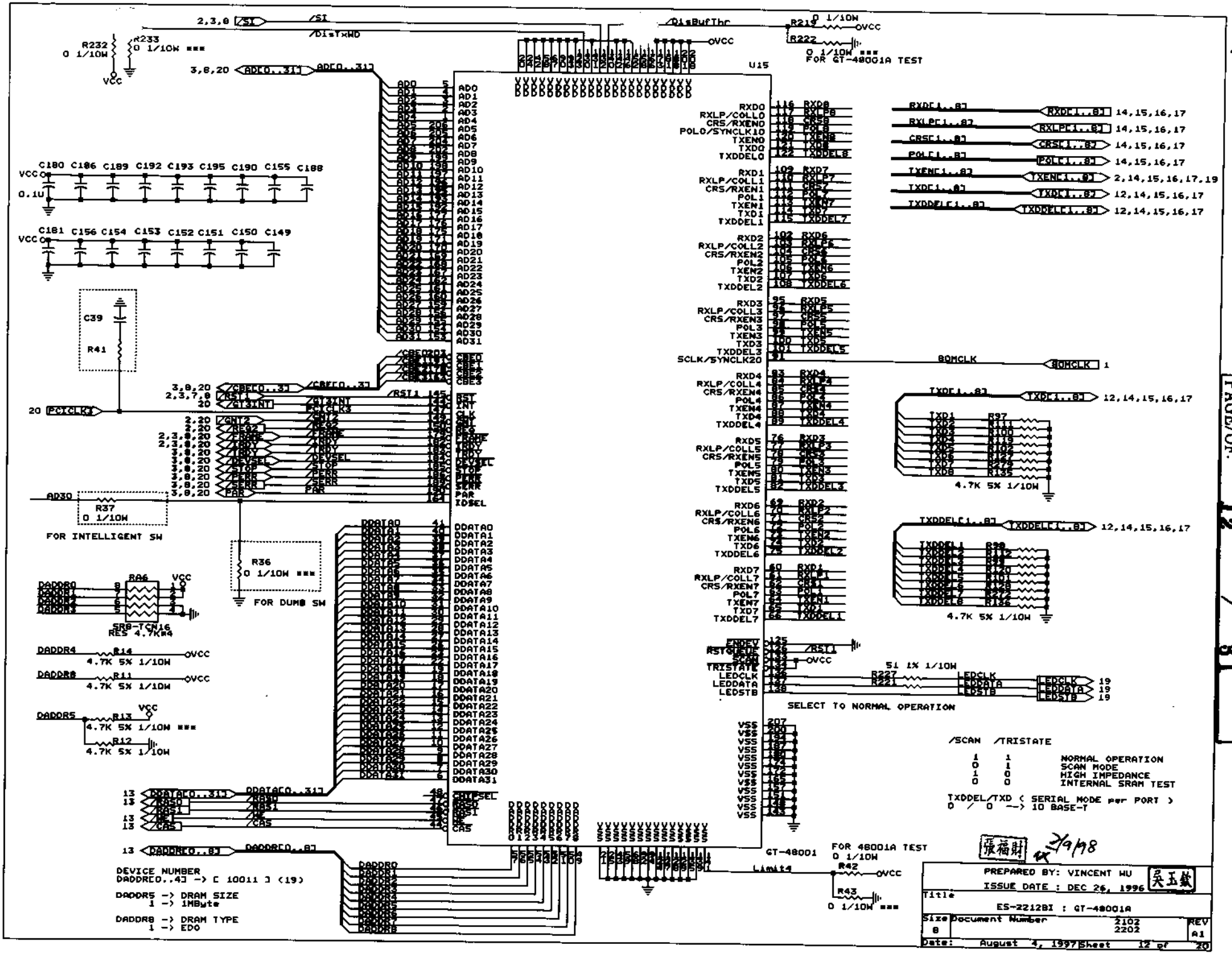
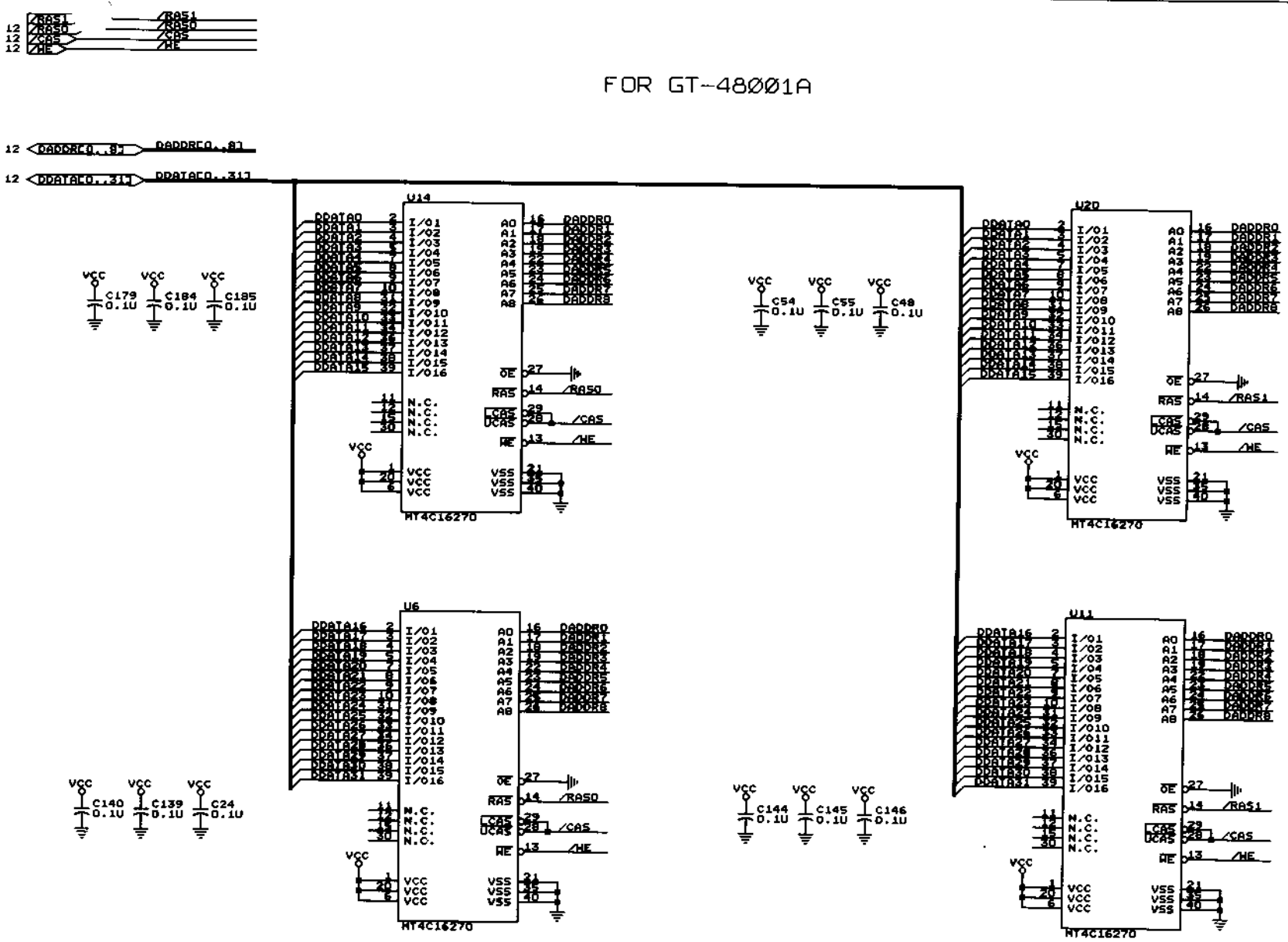
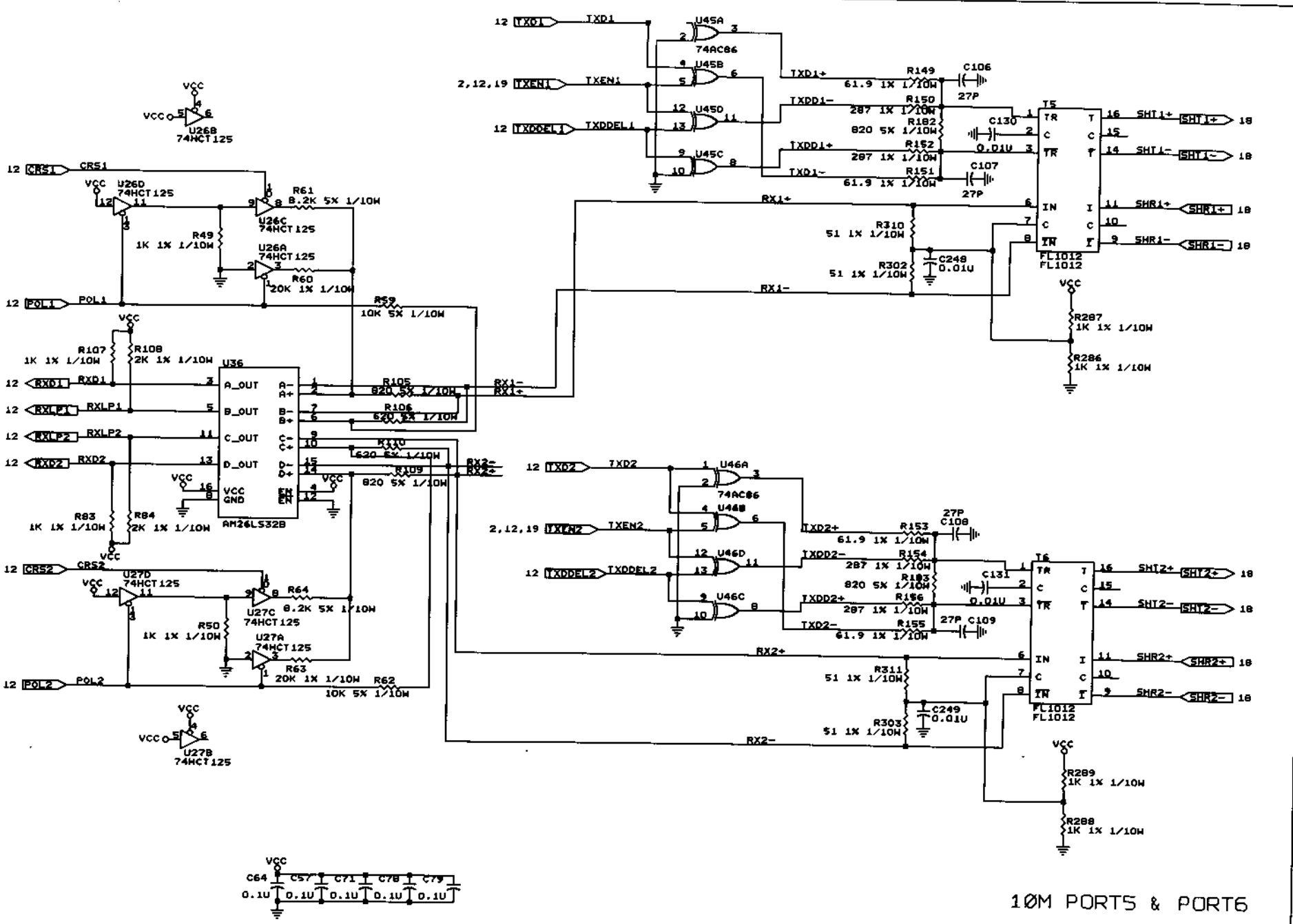


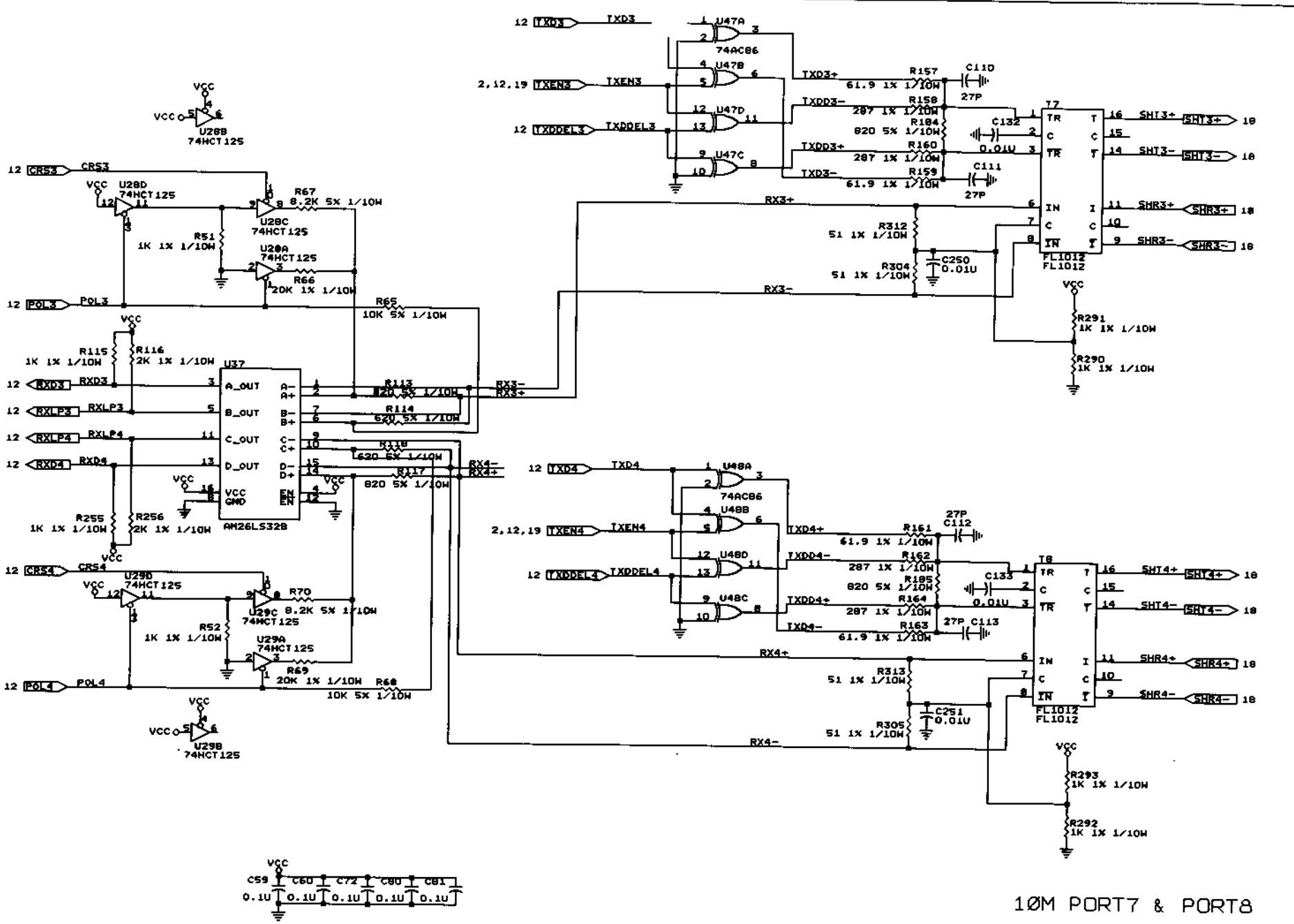
DOC.NO: 305ES2212---A1-
VERSION: A
PAGE/OF: 12 / 81

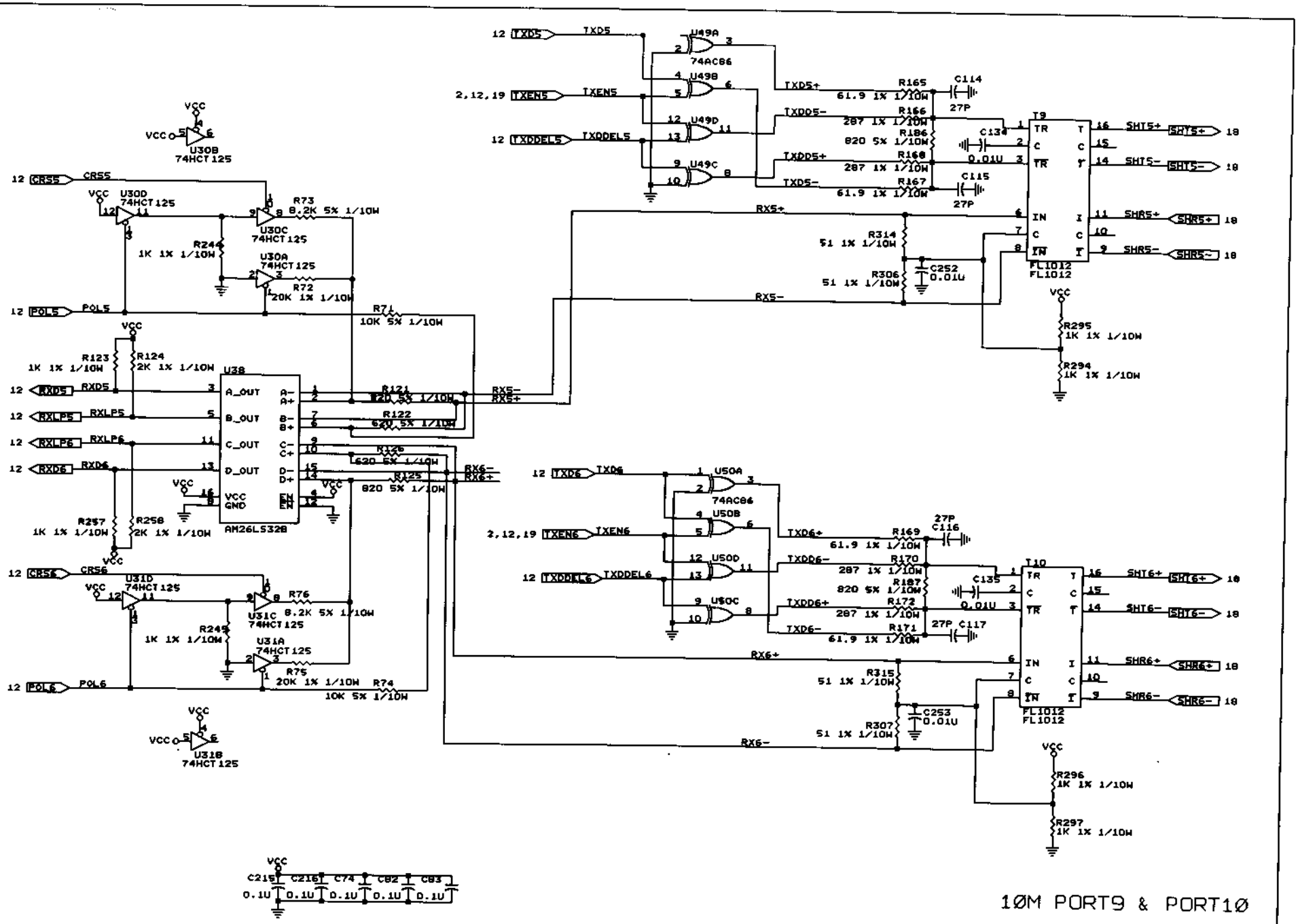


USE 1M BYTE MEMORY.
FOR GT-48001(A)
MEMORY IS 60ns EDO RAM

D-Link Corp.	Approved 張福財	7/9/98	PREPARED BY: VINCENT WU 吳玉欽
	Checked 張福財	7/9/98	ISSUE DATE : DEC 26, 1996
DOC. NO.: 305DES2212---A1-	Version: A		Title ES-2212BI : DRAM FOR GT-48001A
			Size B Document Number 2102 2202 REV A1
			Date: July 16, 1997 Sheet 13 of 20


10M PORT5 & PORT6
D-Link Corp.
Approved: 張福財 3/9/98
Checked: 張福財 3/9/98
PREPARED BY: VINCENT WU 吳玉敏
ISSUE DATE : DEC 26, 1996
Title: ES-2212MI : 10M PORT5 & PORT6 CKT
DOC. NO.: 305DES2212---A1-
Version: A
Size: B
Document Number: 2102 2202
REV: A1
Date: July 21, 1997 Sheet 14 of 20


12 TXD3
2,12,19 TXEN3
12 TXDDEL3
U47A
74AC86
U47B
U47D
U47C
TXD3+
TXDD3-
TXDD3+
TXD3-
R157 61.9 1% 1/10W
R158 287 1% 1/10W
R184 820 5% 1/10W
R160 287 1% 1/10W
R159 61.9 1% 1/10W
C110 27P
C132 0.01U
C111 27P
T7
FL1012
SHT3+
SHT3-
SHR3+
SHR3-
RX3+
RX3-
R312 51 1% 1/10W
R304 51 1% 1/10W
C250 0.01U
R291 1K 1% 1/10W
R290 1K 1% 1/10W
12 TXD4
2,12,19 TXEN4
12 TXDDEL4
U48A
74AC86
U48B
U48D
U48C
TXD4+
TXDD4-
TXDD4+
TXD4-
R161 61.9 1% 1/10W
R162 287 1% 1/10W
R185 820 5% 1/10W
R164 287 1% 1/10W
R163 61.9 1% 1/10W
C112 27P
C133 0.01U
C113 27P
T8
FL1012
SHT4+
SHT4-
SHR4+
SHR4-
RX4+
RX4-
R313 51 1% 1/10W
R305 51 1% 1/10W
C251 0.01U
R293 1K 1% 1/10W
R292 1K 1% 1/10W
12 CRS3
12 POL3
U28D
74HCT125
U28C
U28A
U28B
R67 8.2K 5% 1/10W
R51 1K 1% 1/10W
R66 20K 1% 1/10W
R65 10K 5% 1/10W
R115 1K 1% 1/10W
R116 2K 1% 1/10W
U37
AM26LS32B
12 RXD3
12 RXLP3
12 RXLP4
12 RXD4
R113 620 5% 1/10W
R114 620 5% 1/10W
R118 620 5% 1/10W
R117 820 5% 1/10W
R255 1K 1% 1/10W
R256 2K 1% 1/10W
12 CRS4
12 POL4
U29D
U29C
U29A
U29B
R70 8.2K 5% 1/10W
R52 1K 1% 1/10W
R69 20K 1% 1/10W
R68 10K 5% 1/10W
C59 0.1U
C60 0.1U
C72 0.1U
C80 0.1U
C81 0.1U
10M PORT7 & PORT8
D-Link Corp.
Approved 張福財 2/9/98
Checked 張福財 2/9/98
PREPARED BY: VINCENT WU 吳玉敏
ISSUE DATE : DEC 26, 1996
Title ES-2212BI : 10M PORT7 & PORT8 CKT
DOC. NO.: 305DES2212---A1-
Version: A
Size B
Document Number 2102 2202
REV A1
Date: July 21, 1997 Sheet 15 of 20


12 TXD5
TXD5
U49A
74AC86
2,12,19 TXEN5
TXEN5
U49B
12 TXDDEL5
TXDDEL5
U49D
U49C
TXD5+
TXDD5-
TXDD5+
TXD5-
R165 61.9 1% 1/10W
R166 287 1% 1/10W
R186 820 5% 1/10W
R168 287 1% 1/10W
R167 61.9 1% 1/10W
C114 27P
C134 0.01U
C115 27P
T9
FL1012
SHT5+
SHT5-
SHR5+
SHR5-
RX5+
RX5-
R314 51 1% 1/10W
R306 51 1% 1/10W
C252 0.01U
R295 1K 1% 1/10W
R294 1K 1% 1/10W
VCC
U30B 74HCT125
12 CRS5
CRS5
U30D 74HCT125
U30C 74HCT125
U30A 74HCT125
R73 8.2K 5% 1/10W
R24 1K 1% 1/10W
R72 20K 1% 1/10W
12 POL5
POL5
R71 10K 5% 1/10W
R123 1K 1% 1/10W
R124 2K 1% 1/10W
U38
AM26LS32B
12 RXD5
RXD5
12 RXLP5
RXLP5
12 RXLP6
RXLP6
12 RXD6
RXD6
A_OUT
B_OUT
C_OUT
D_OUT
VCC
GND
R121 820 5% 1/10W
R122 820 5% 1/10W
R126 820 5% 1/10W
R125 820 5% 1/10W
RX6-
RX6+
R257 1K 1% 1/10W
R258 2K 1% 1/10W
12 CRS6
CRS6
U31D 74HCT125
U31C 74HCT125
U31A 74HCT125
R76 8.2K 5% 1/10W
R245 1K 1% 1/10W
R75 20K 1% 1/10W
12 POL6
POL6
R74 10K 5% 1/10W
U31B 74HCT125
12 TXD6
TXD6
U50A
74AC86
2,12,19 TXEN6
TXEN6
U50B
12 TXDDEL6
TXDDEL6
U50D
U50C
TXD6+
TXDD6-
TXDD6+
TXD6-
R169 61.9 1% 1/10W
R170 287 1% 1/10W
R187 820 5% 1/10W
R172 287 1% 1/10W
R171 61.9 1% 1/10W
27P C116
C135 0.01U
27P C117
T10
FL1012
SHT6+
SHT6-
SHR6+
SHR6-
R315 51 1% 1/10W
R307 51 1% 1/10W
C253 0.01U
R296 1K 1% 1/10W
R297 1K 1% 1/10W
C215 0.1U
C216 0.1U
C74 0.1U
C82 0.1U
C83 0.1U
10M PORT9 & PORT10
D-Link Corp.
Approved
Checked:
PREPARED BY: VINCENT WU
ISSUE DATE : DEC 26, 1996
Title
ES-2212BI : 10M PORT9 & PORT10 CKT
DOC. NO.: 305DES2212---A1-
Version: A
Size: B
Document Number 2102 2202
REV A1
Date: July 21, 1997 Sheet 16 of 20

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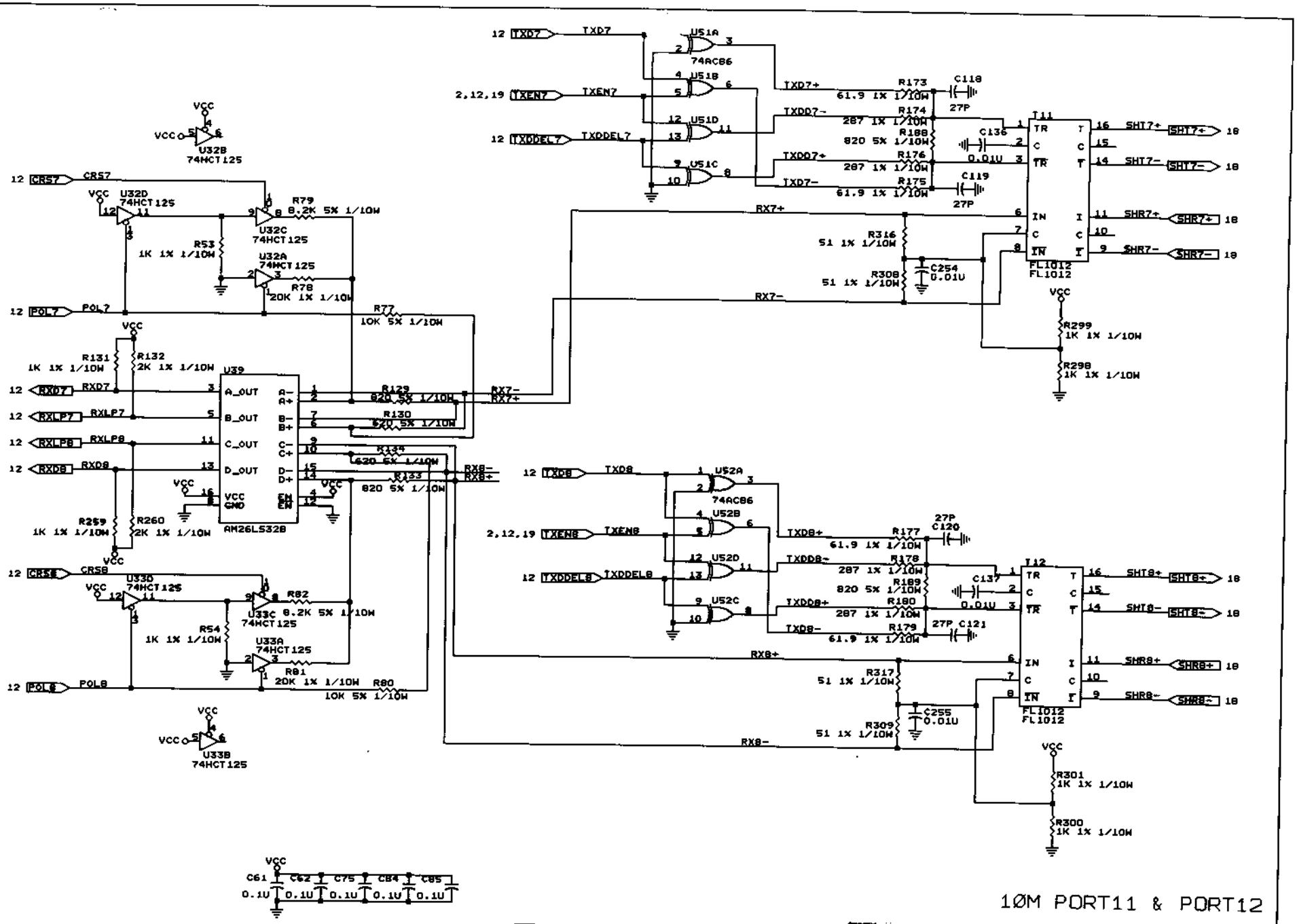
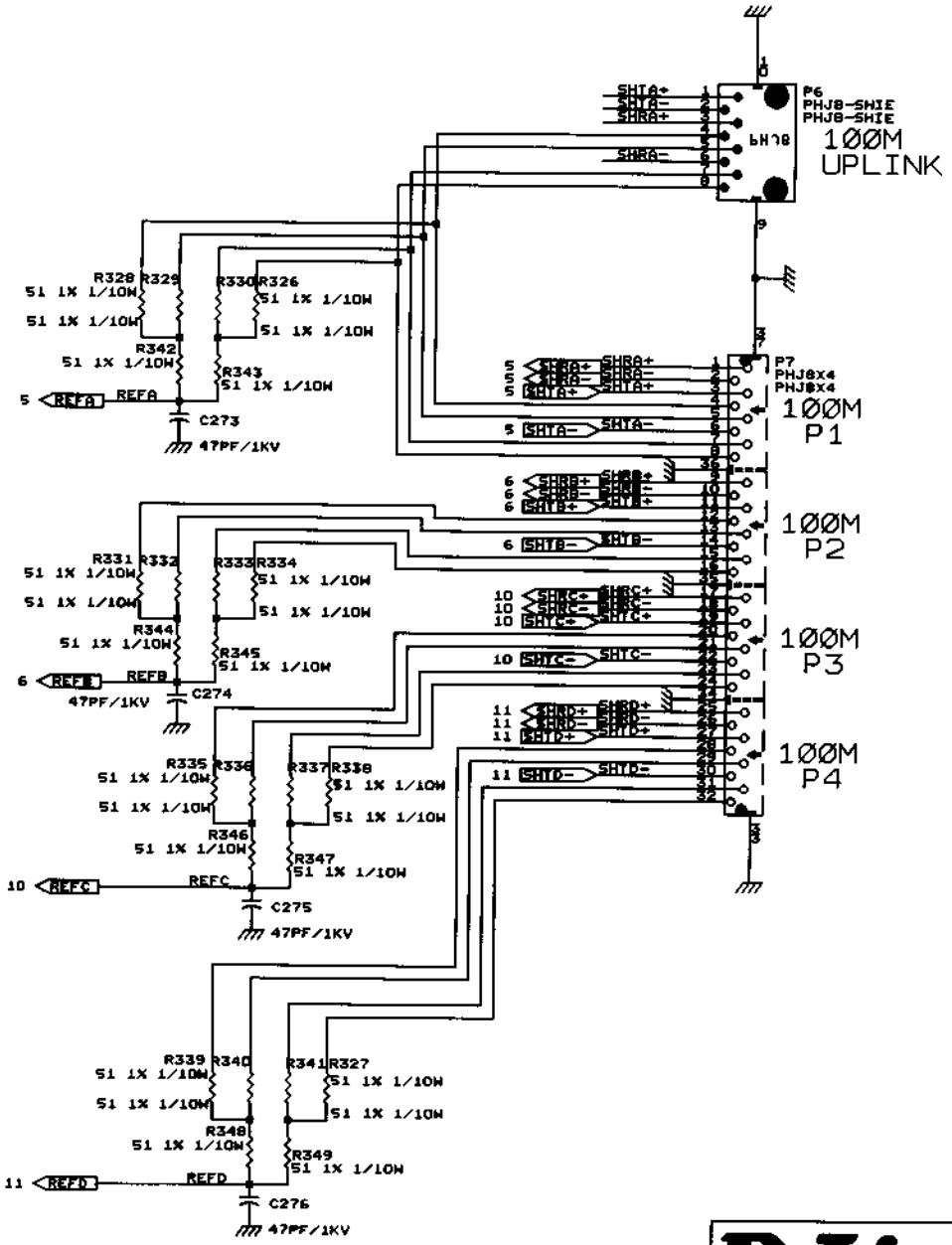
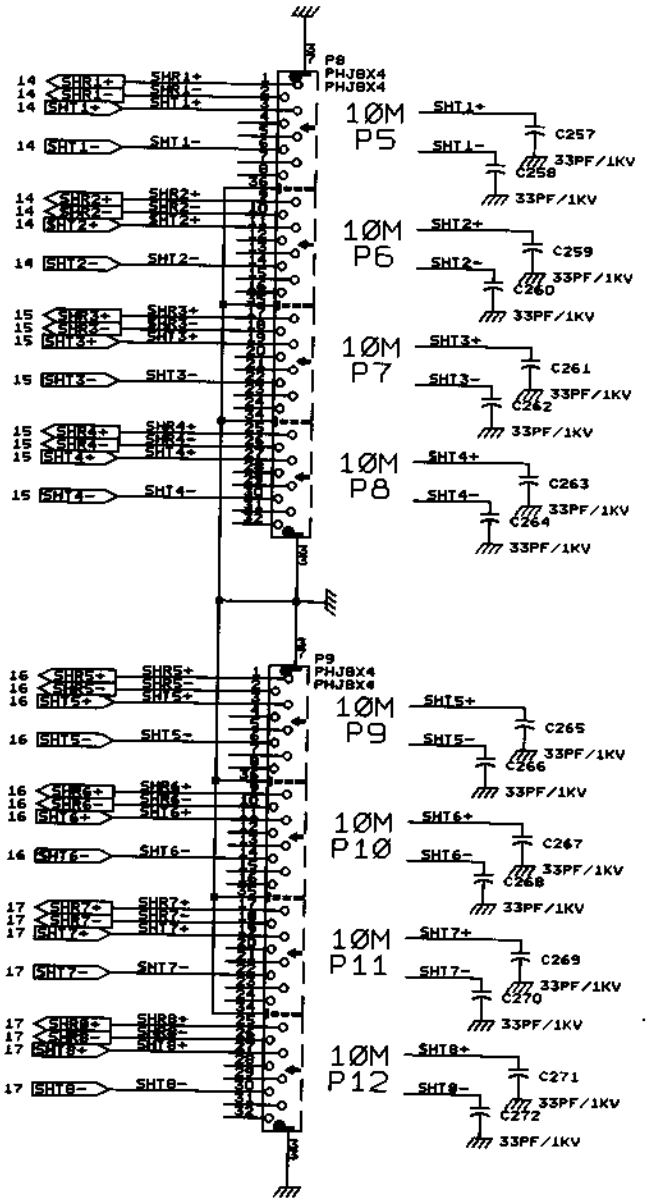


10M PORT11 & PORT12

D-Link Corp.

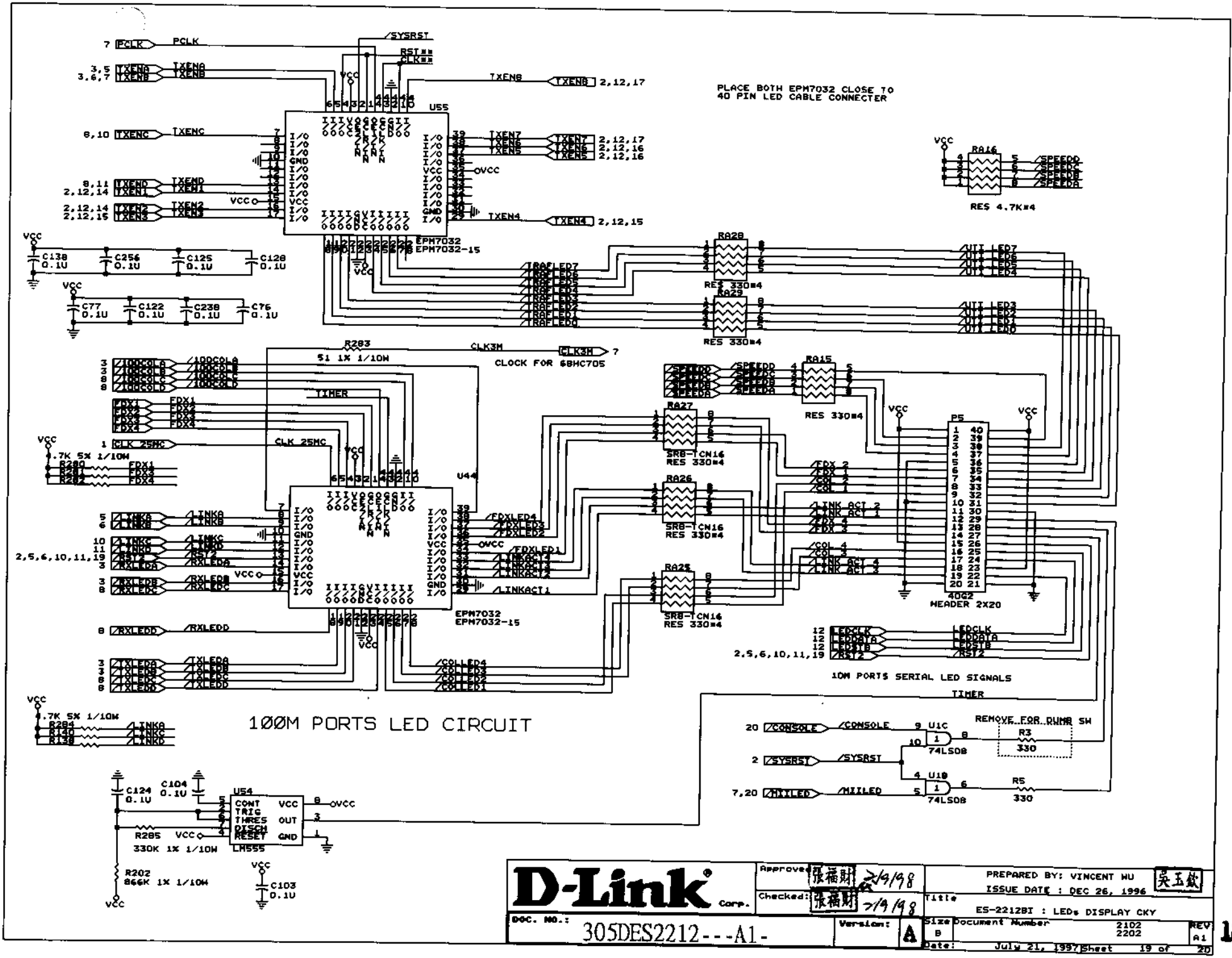
Approved: 張福財 2/9/98	PREPARED BY: VINCENT WU 吳玉敏		
Checked: 張福財 2/9/98	ISSUE DATE : DEC 26, 1996		
DOC. NO.: 305DES2212---A1-	Version: A	Title: ES-2212BI : 10M PORT11 & PORT12 CKT	
		Size: B Document Number: 2102 2202	REV: A1
		Date: July 21, 1997 Sheet 17 of 20	





100M & 10M PHONE JACKS

D-Link Corp.	Approved: 張福財 3/9/98	PREPARED BY: VINCENT WU 吳玉敏	
	Checked: 張福財 3/9/98	ISSUE DATE : DEC 26, 1996	
DOC. NO.: 305DES2212---A1-	Version: A	Title: ES-2212BI : PHONE JACKS	
		Size: B Document Number: 2102 2202	REV: A1
		Date: July 16, 1997 Sheet 18 of 20	



D-Link Corp.	Approved: 張福財 2/9/98	PREPARED BY: VINCENT WU 吳玉欽	
	Checked: 張福財 2/9/98	ISSUE DATE : DEC 26, 1996	
DOC. NO.: 305DES2212---A1-	Version: A	Title: ES-2212BI : LEDs DISPLAY CKY	
		Size: B Document Number: 2102 2202 REV: A1	
		Date: July 21, 1997 Sheet 19 of 20	

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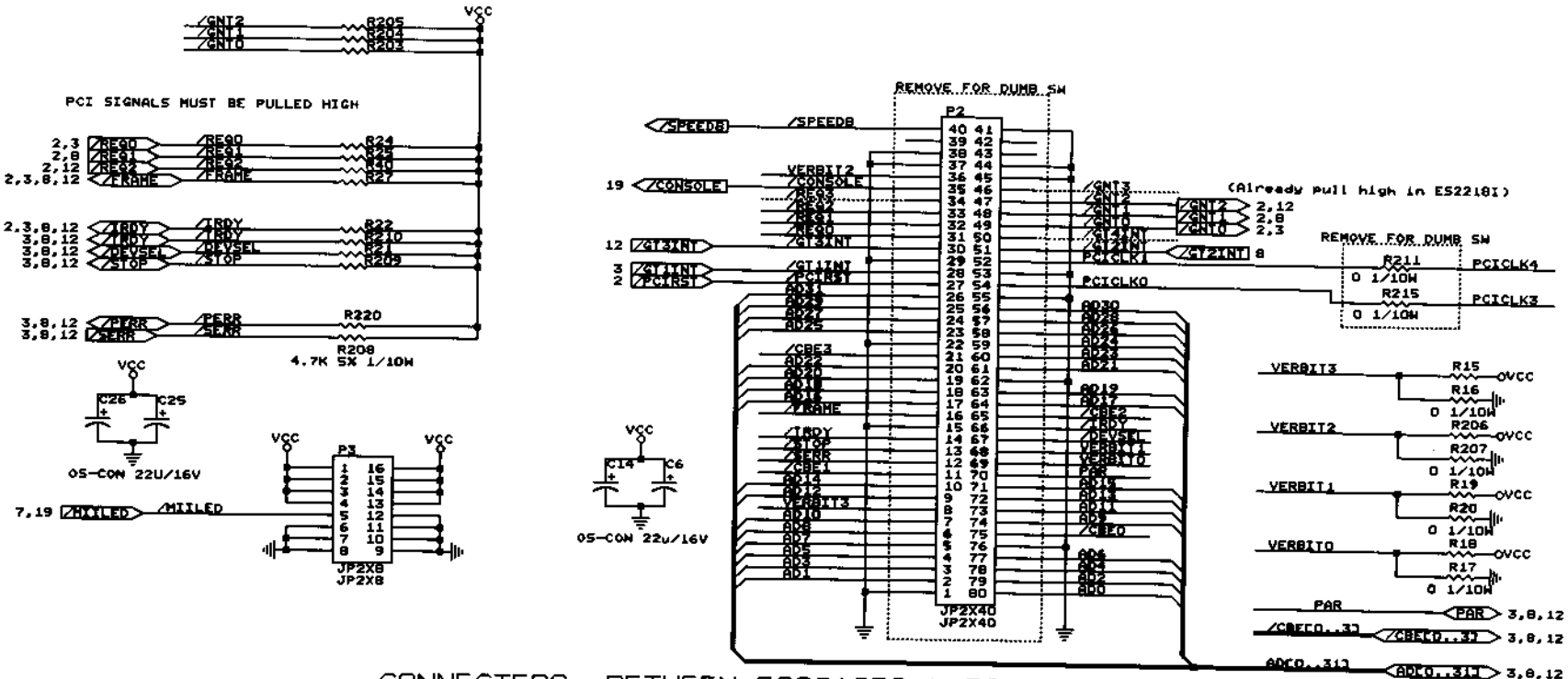
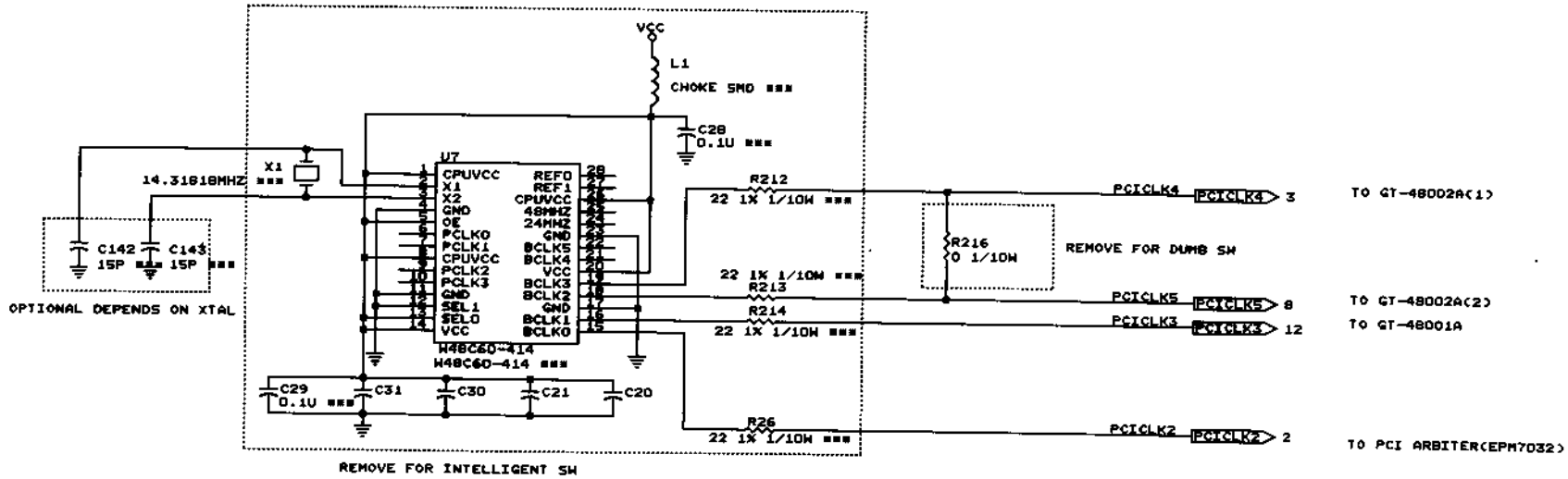
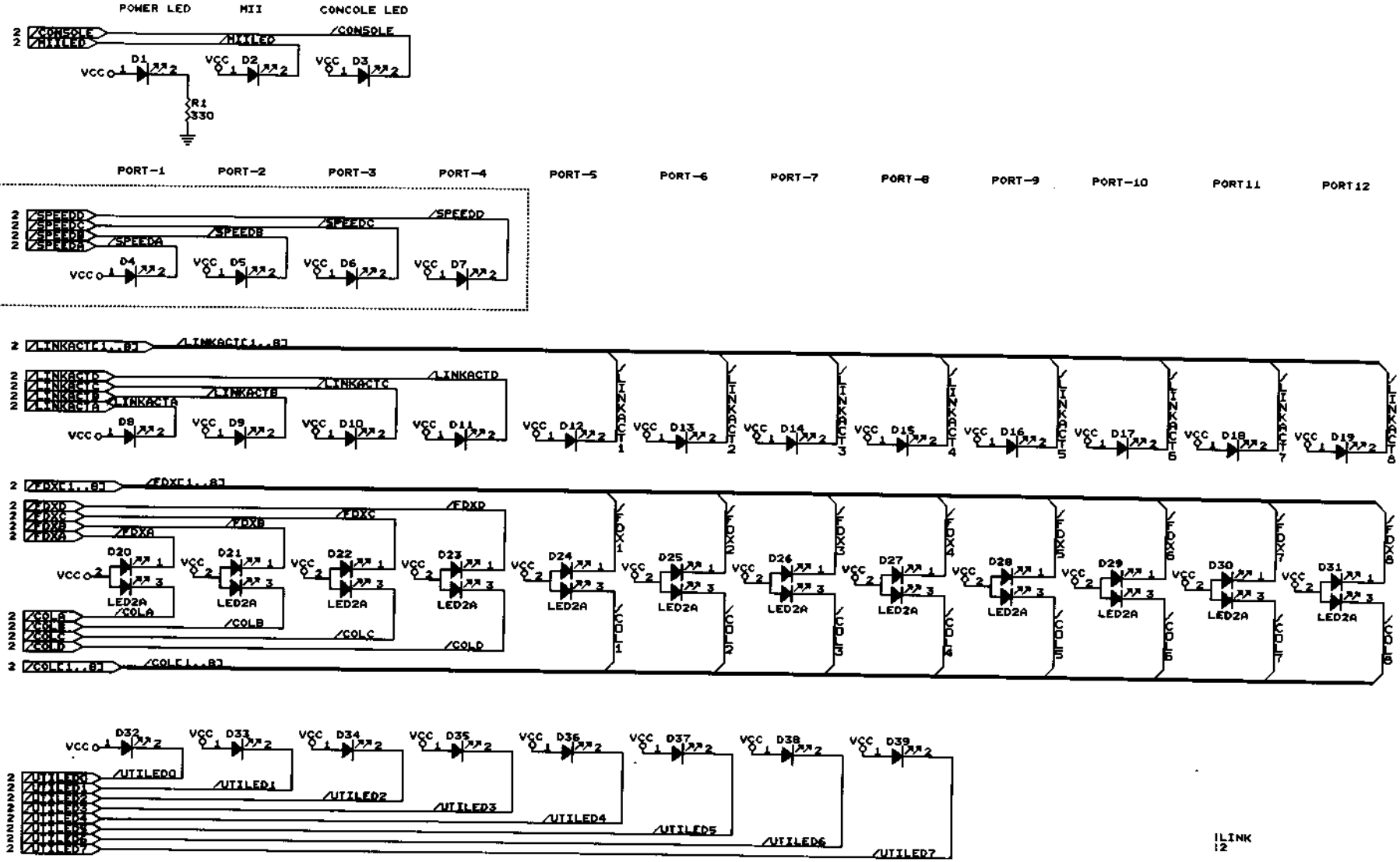


CONNECTERS BETWEEN ES2212BI & ES2218I



PCI CLOCK (33M) GENERATION FOR DUMB SW

D-Link Corp.	Approved: 張福財 2/9/98	PREPARED BY: VINCENT WU 吳玉鉞	
	Checked: 張福財 2/9/98	ISSUE DATE : DEC 26, 1996	
DOC. NO.: 305DES2212---A1-	Version: A	Title: ES-2212BI : B2B CONN. & PCI CLOCKS	
		Size: B Document Number: 2102 2202	REV: A1
		Date: July 21, 1997 Sheet 20 of 20	



PORT TRAFFIC LED

15.2 X 11.7

D-Link Corp.	Approved: 張福財 3/9/98	PREPARED BY: VINCENT WU	
	Checked: 張福財 3/9/98	ISSUE DATE : JULY 7, 1997	
		Title	ES-2212L : LEDs ARRAY
DOC. NO.: 305DES2212---A1-	Version: A	Size B	Document Number 2103 2203 REV A1
		Date: August 6, 1997	Sheet 1 of 2

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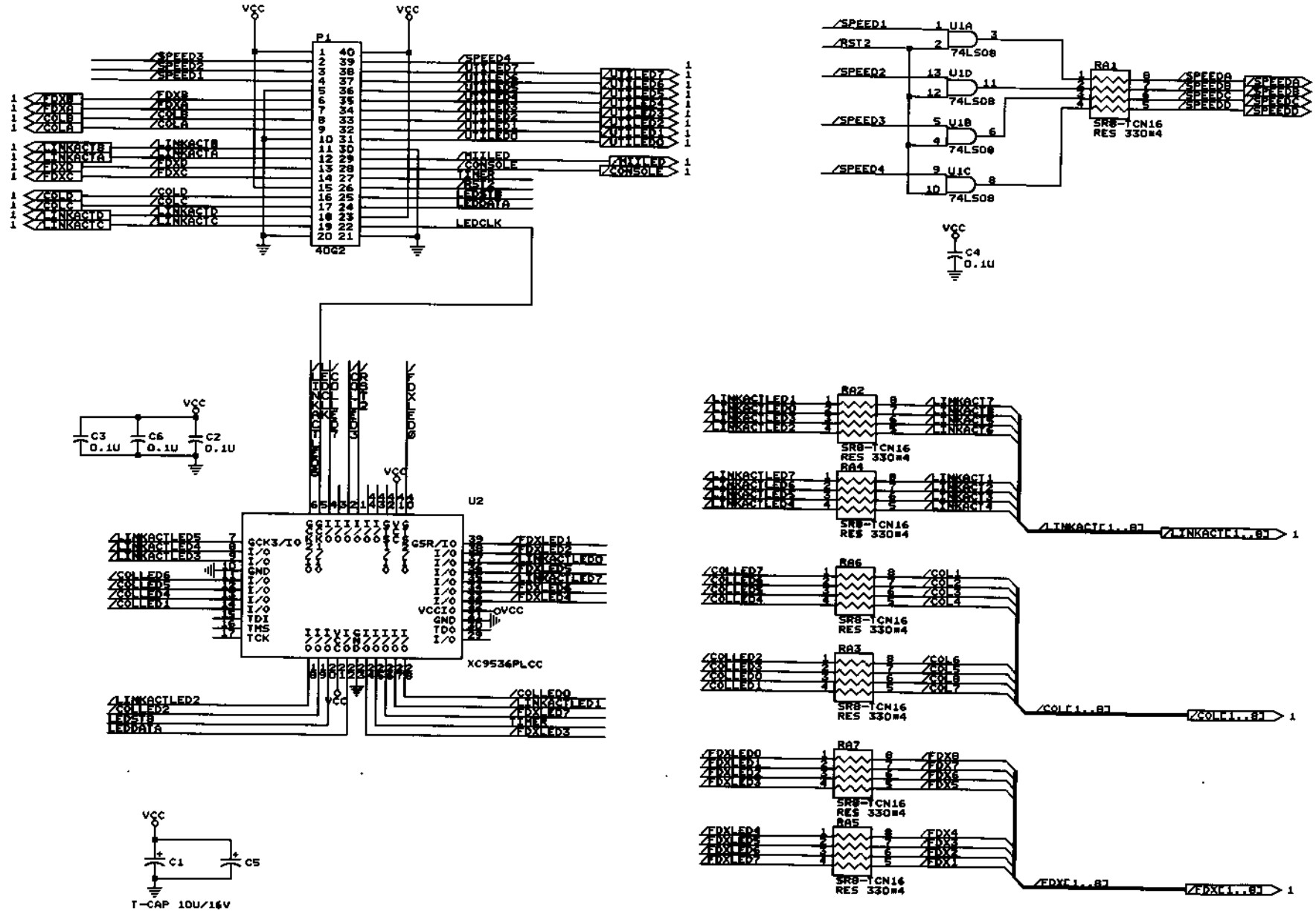
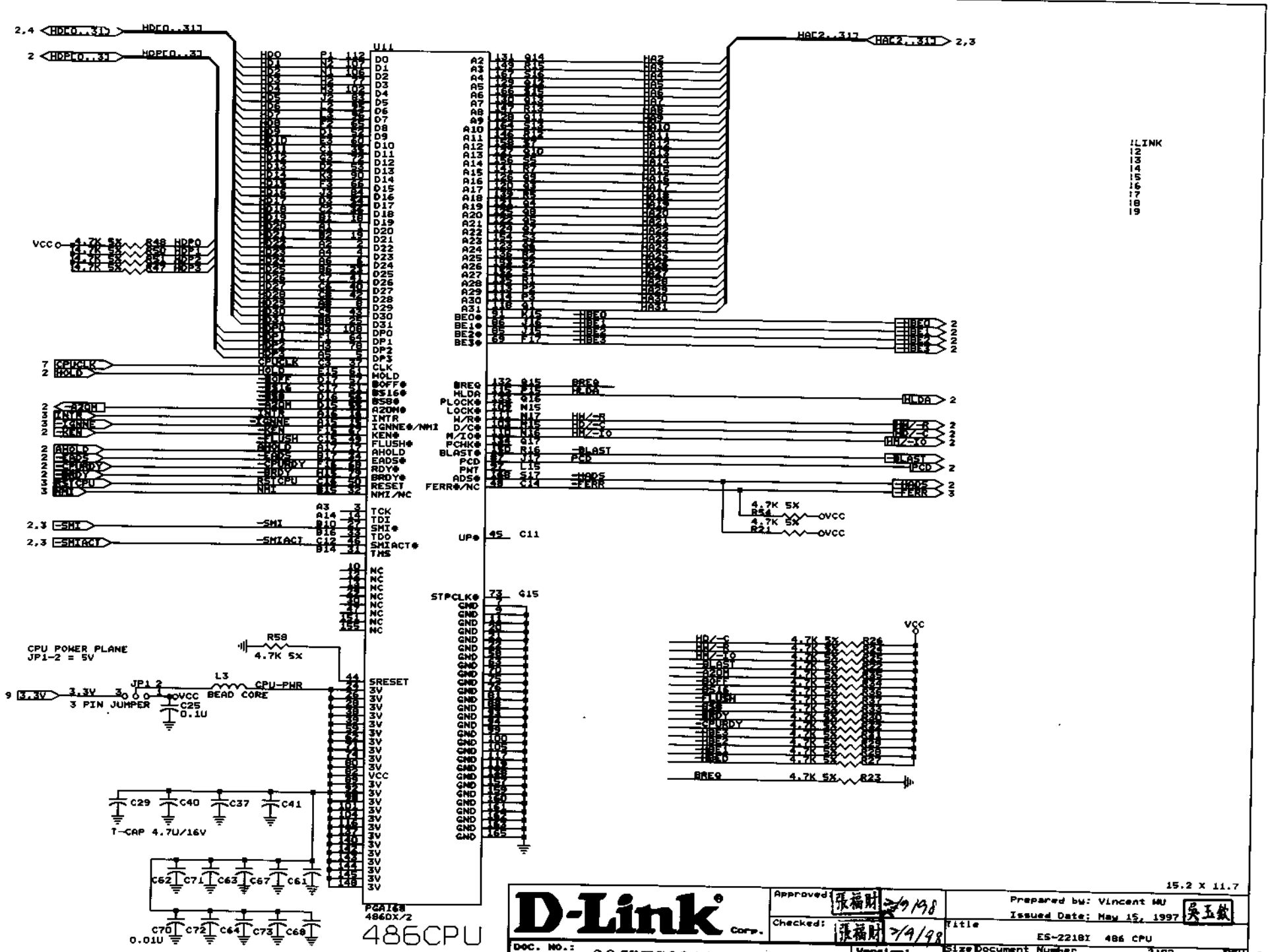
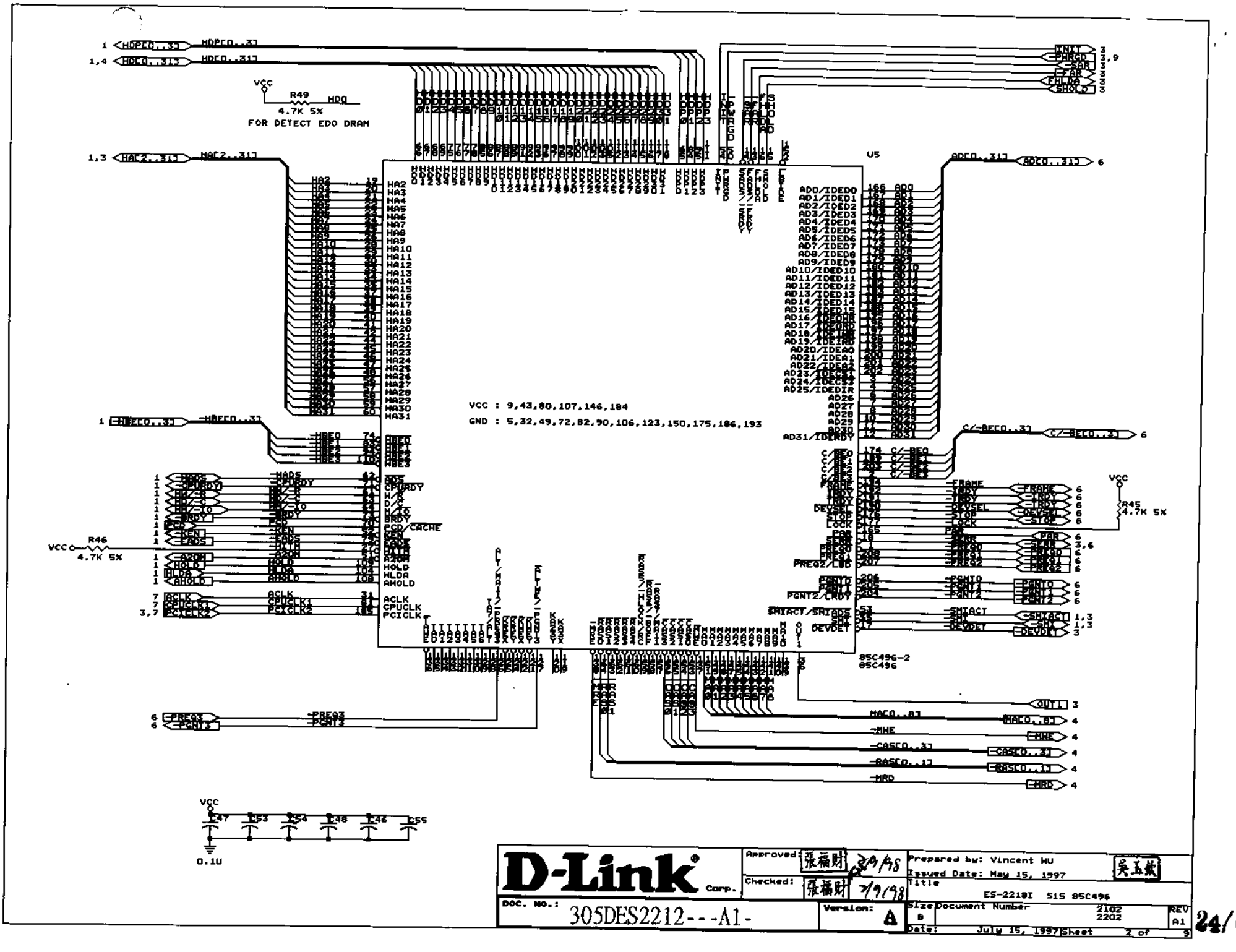

P1
40G2
U2
XC9536PLCC
74LS08
SR8-TCN16
RES 330*4
T-CAP 10U/16V
D-Link Corp.
PREPARED BY: VINCENT WU
ISSUE DATE : JULY. 7, 1997
Approved
Checked
Title
ES-2212L : LED CABLE CONN. & DECODE CKT
DOC. NO.: 305DES2212---A1-
Version: A
Size: B
Document Number: 2103 2203
REV: A1
Date: August 6, 1997 Sheet 2 of 2
15.2 X 11.7


U11
PGA168
486DX/2
486CPU
CPU POWER PLANE
JP1-2 = 5V
3 PIN JUMPER
CPU-PWR
BEAD CORE
T-CAP 4.7U/16V
!LINK
Approved:
Checked:
Prepared by: Vincent HU
Issued Date: May 15, 1997
Title
ES-2218I 486 CPU
DOC. NO.:
305DES2212---A1-
Version:
A
Size
B
Document Number
2102
2202
REV
A1
Date:
July 15, 1997
Sheet
1 of
9
15.2 X 11.7



D-Link Corp.	Approved: 張福財 98/9/8	Prepared by: Vincent WU 吳玉斌	
	Checked: 張福財 7/9/98	Issued Date: May 15, 1997	
		Title: ES-2210I SiS 85C496	
DOC. NO.: 305DES2212---A1-	Version: A	Size: B Document Number: 2102 2202	REV: A1
		Date: July 15, 1997 Sheet 2 of 9	

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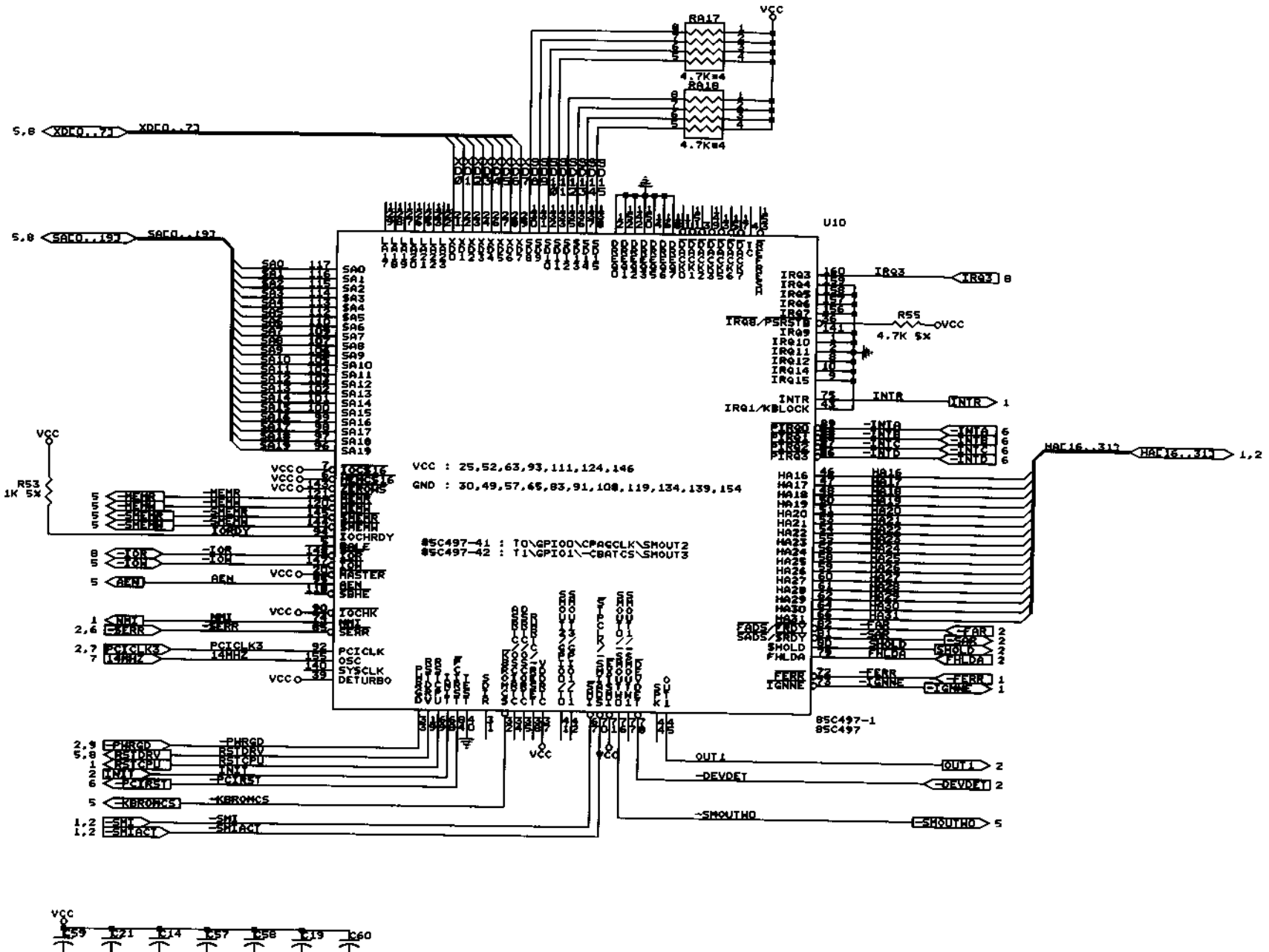

D-Link Corp.	Approved: 張福財 2/9/98	Prepared by: Vincent HU 吳玉欽	
	Checked: 張福財 2/9/98	Issued Date: May 15, 1997	
DOC. NO.: 305DES2212---A1-	Version: A	Title: ES-2218I SiS 85C497	
		Size: B Document Number: 2102 2202	REV: A1
		Date: July 15, 1997 Sheet 3 of 9	

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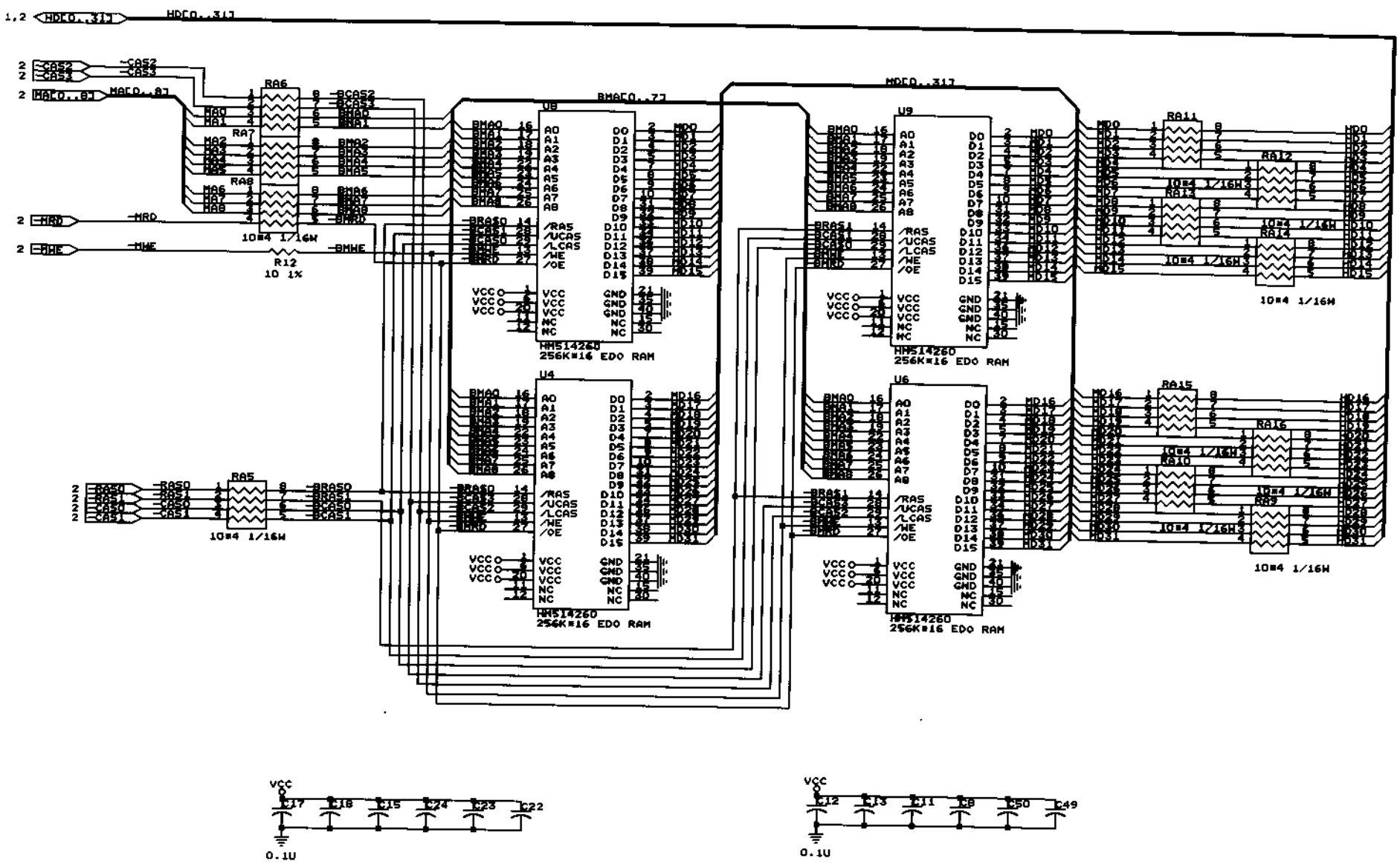
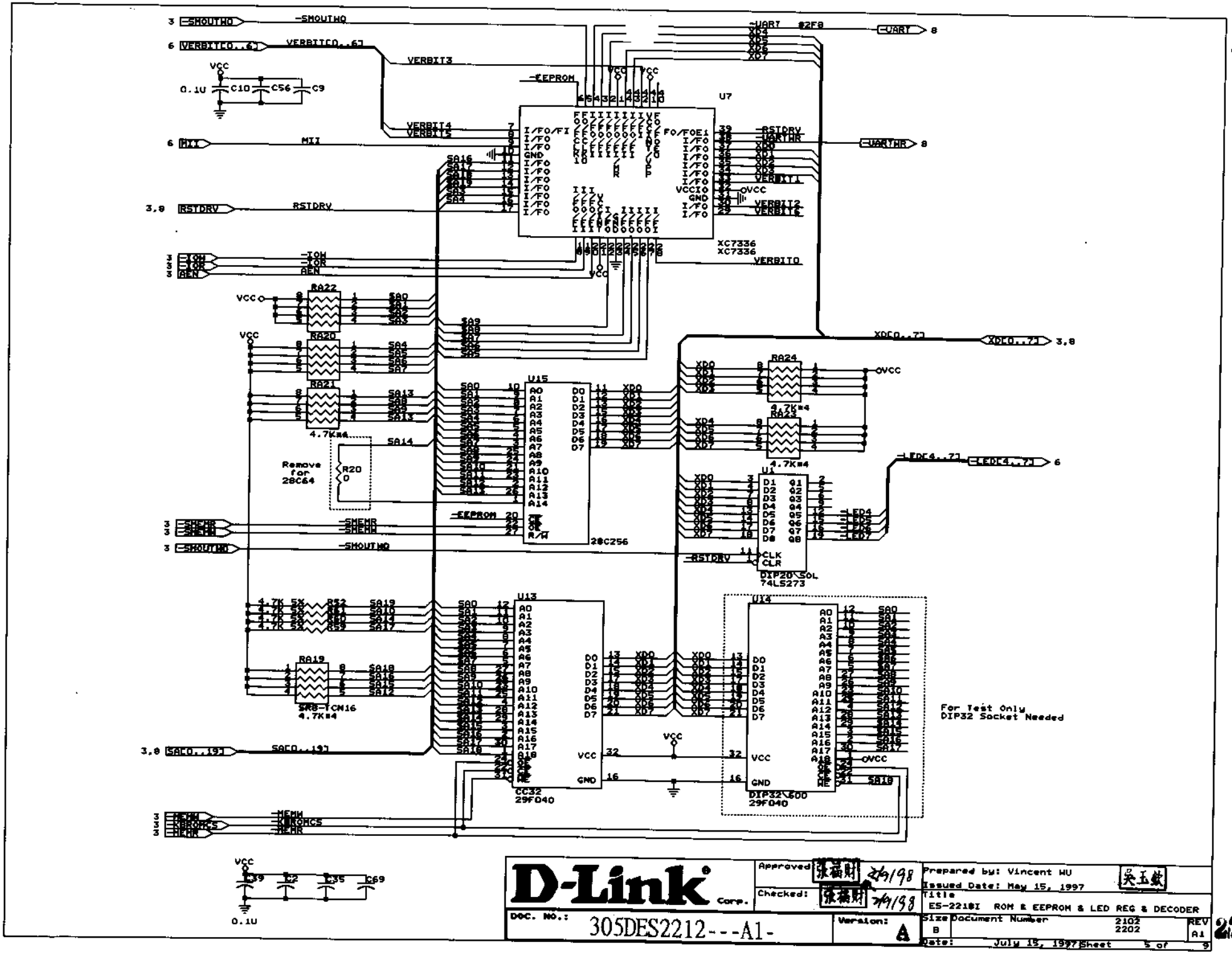
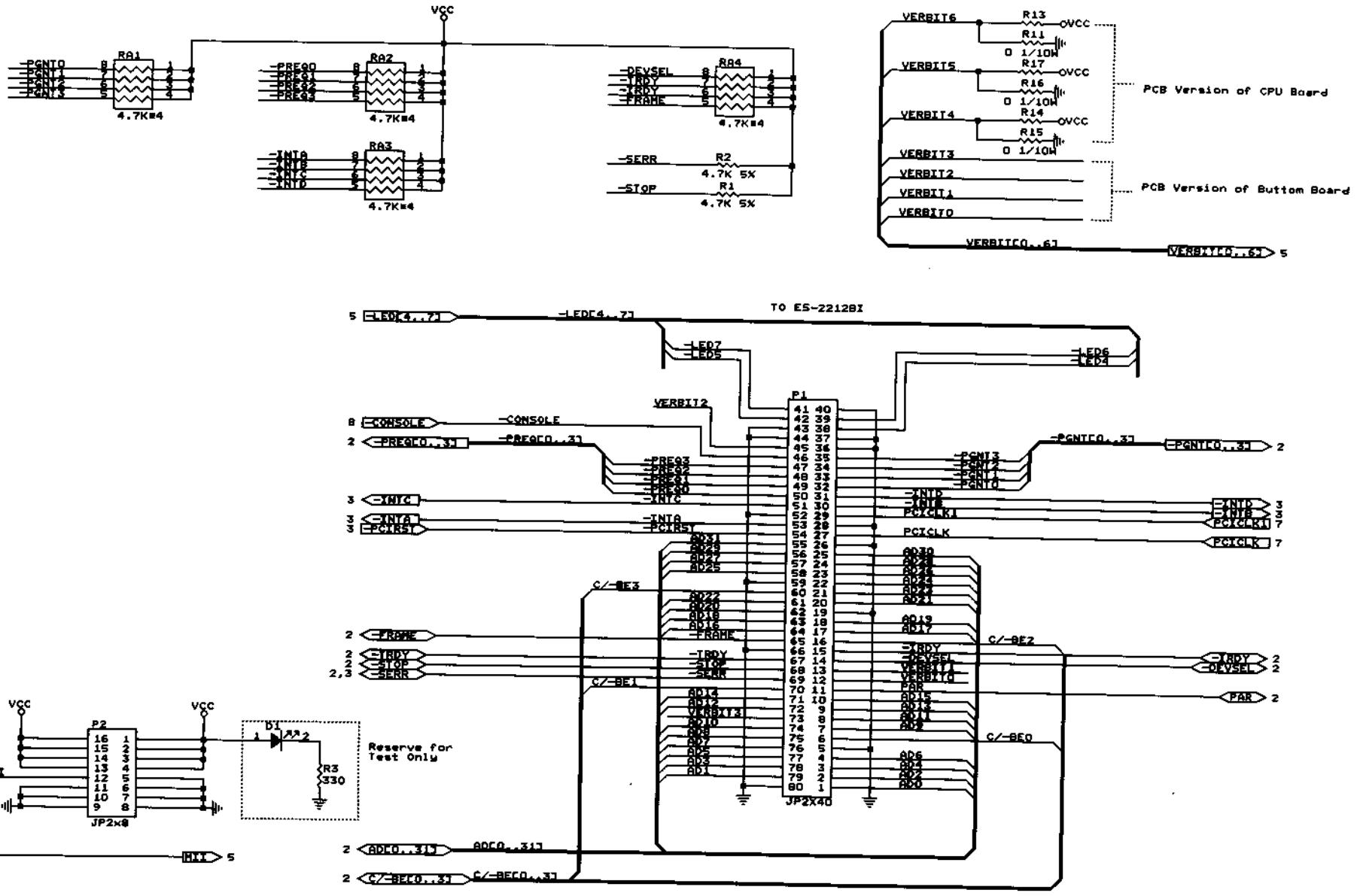


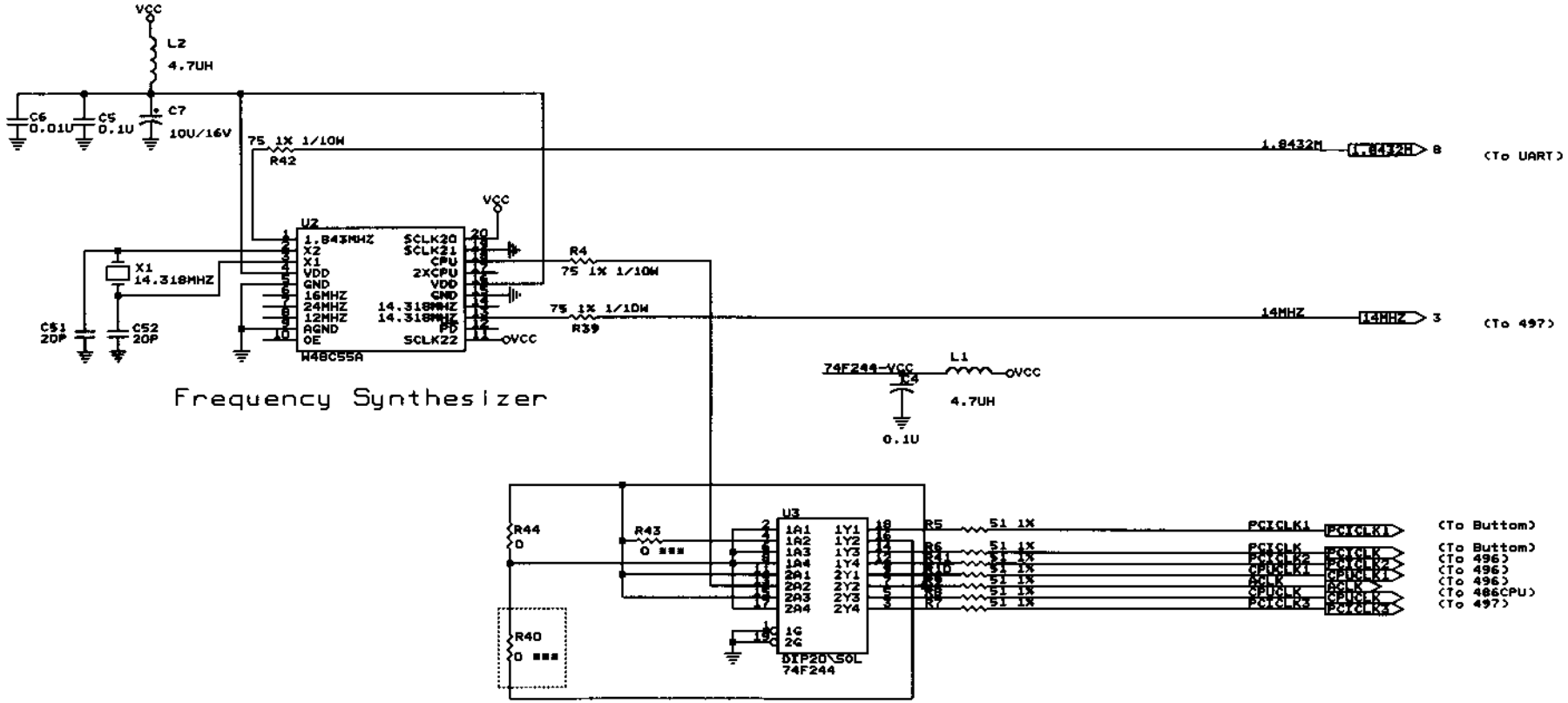
D-Link Corp.	Approved: 張福財 2/9/98	Prepared by: Vincent HU 吳玉鈸	
	Checked: 張福財 2/9/98	Issued Date: May 15, 1997	
		Title: ES-2218I DRAM	
DOC. NO.: 305DES2212---A1-	Version: A	Size: B Document Number: 2102 2202	REV: A1
		Date: July 15, 1997 Sheet 4 of 9	



D-Link Corp.	Approved: 張福財 2/9/98	Prepared by: Vincent WU	吳玉敏
	Checked: 張福財 2/9/98	Issued Date: May 15, 1997	
		Title: ES-2218I ROM & EEPROM & LED REG & DECODER	
DOC. NO.: 305DES2212---A1-	Version: A	Size: B Document Number: 2102 2202	REV: A1
		Date: July 15, 1997 Sheet 5 of 9	



D-Link Corp.	Approved: 張福財 2/9/98	Prepared by: Vincent HU 吳玉欽	
	Checked: 張福財 2/9/98	Issued Date: May 15, 1997	
DOC. NO.: 305DES2212---A1-	Version: A	Title: ES-2218I B28 PCI CONNECTOR	
		Size: B Document Number: 2102 2202	REV: A1
		Date: July 15, 1997 Sheet 6 of 9	



Frequency Synthesizer

Clock Driver for 33MHz

D-Link Corp.	Approved: 張福財 2/9/98	Prepared by: Vincent WU 吳玉成	
	Checked: 張福財 2/9/98	Issued Date: May 15, 1997	
		Title: ES-2218I SYSTEM CLOCKS GENERATION	
DOC. NO.: 305DES2212---A1-	Version: A	Size: B Document Number: 2102 2202	REV: A1
		Date: July 15, 1997 Sheet 7 of 9	

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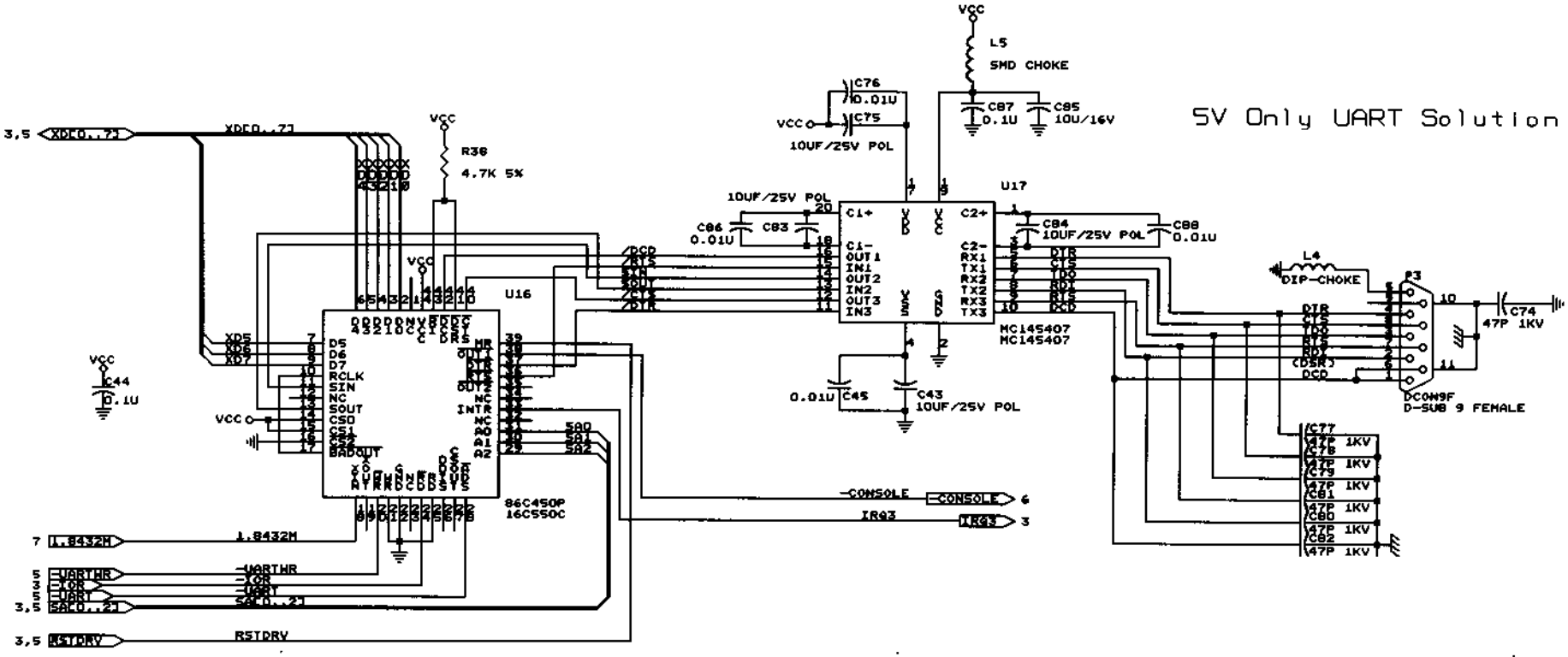

D-Link Corp.	Approved: 張福財 2/9/98	Prepared by: Vincent WU		
	Checked: 張福財 2/9/98	Issued Date: May 15, 1997		
		Title: ES-2218I CONSOLE PORT		
DOC. NO.: 305DES2212---A1-	Version: A	Size: B	Document Number: 2102 2202	REV: A1
		Date: July 15, 1997	Sheet 8 of 9	

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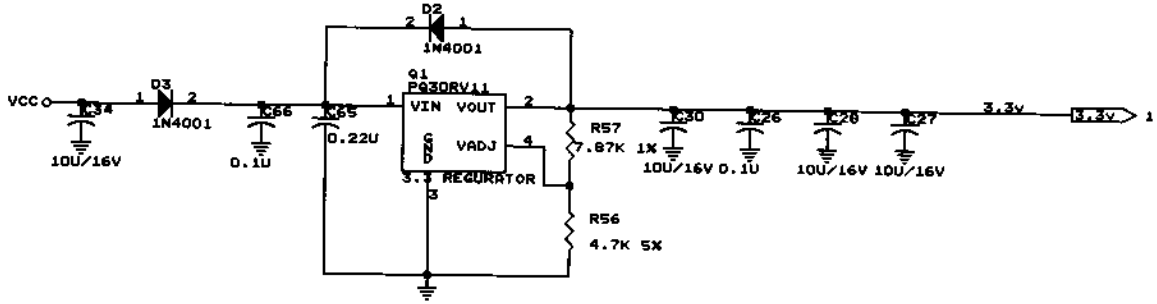
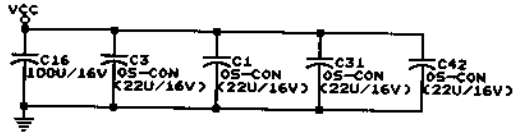
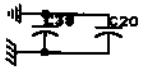
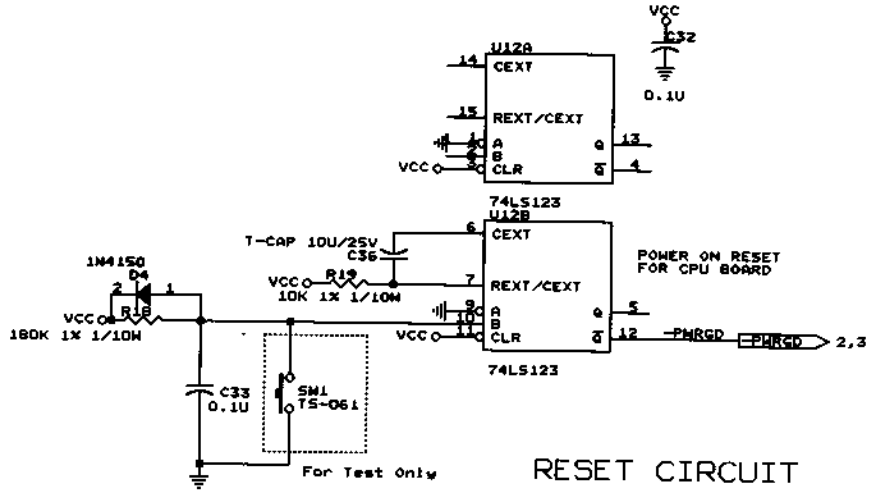


5V -> 3.3V POWER CONVERSION







RESET CIRCUIT

D-Link Corp.	Approved: 梁福財 7/9/98	Prepared by: Vincent WU 吳玉鼓	
	Checked: 梁福財 7/9/98	Issued Date: May 15, 1997	
		Title: ES-2210I POWER & RESET	
DOC. NO.: 305DES2212---A1-	Version: A	Size: B Document Number: 2102 2202	REV: A1
		Date: July 15, 1997 Sheet 9 of 9	

生效日期: 87. 2. 26

REV DATE:	
ISSUED DATE:	87. 2. 26
DOC.NO.	305DES2212---A1-
VERSION	A
PAGE/OF	0 / 81

文 件 履 歷 表

DES-2212 A1 CKT Diagram

修訂日期	版本	變 更 內 容
87. 2. 26	A	Refer NPR DES 2212 --- A1-01