

CHILD

生效日期: 87. 4. 30

DZ5810 Rev. A2


家 國

[illegible]

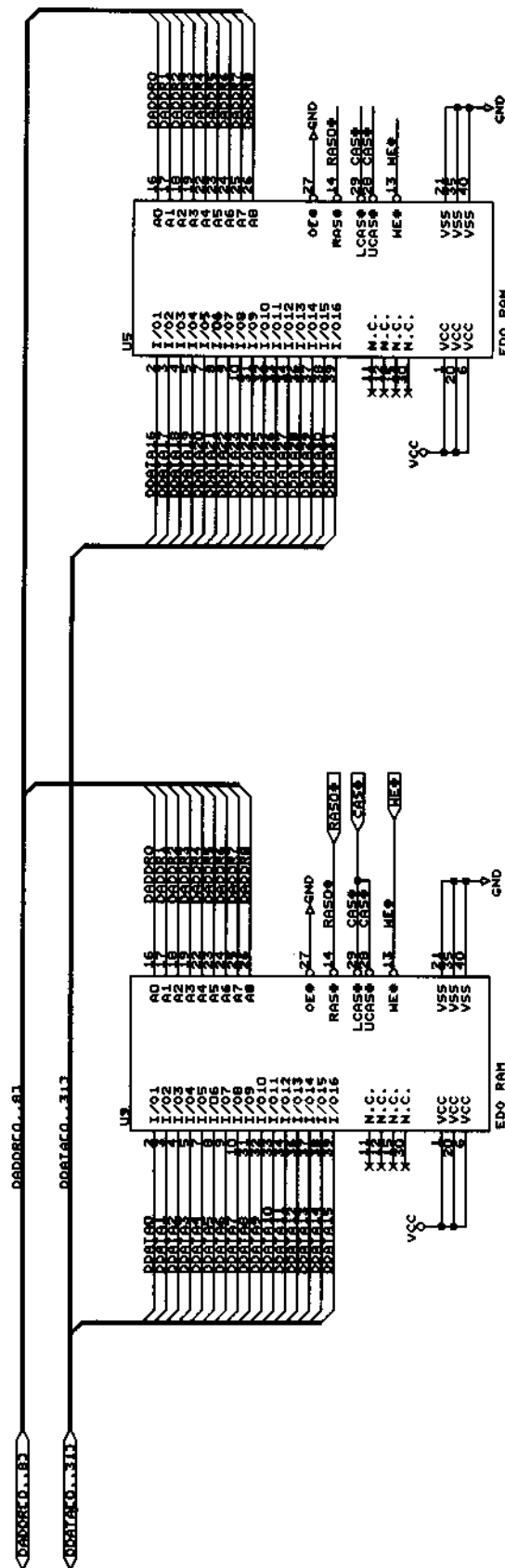
APPROVED	CHECKED	DEPARTMENT	PREPARED
30. 10. 1950	10. 10. 1950		P. 11. 1950

86/05/c

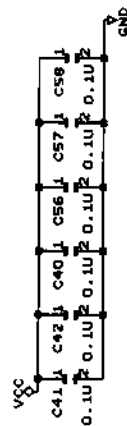


D-Link® DOC. NO.: 305DES810 --- A2-		Approved:  陳志才 C. Chai	Prepared: POLLY PAN Issued Date: 20/98 Title: DES-810/DES-818's LOW PCB
Version: A		Size: 8 Document Number: 0EM-0000-00-V10	REV: A2 Date: February 16, 1998 Sheet 2 of 21

DRAM FOR GT48001



USE 1M BYTE MEMORY
MEMORY IS 60ns EDO DRAM



D-Link

Approved: *Chen* 1/19/98

Prepared: POLLY PAN

Issued Date:

Title: DES-810/DES-818's LOW_PCB

Size Document Number: B

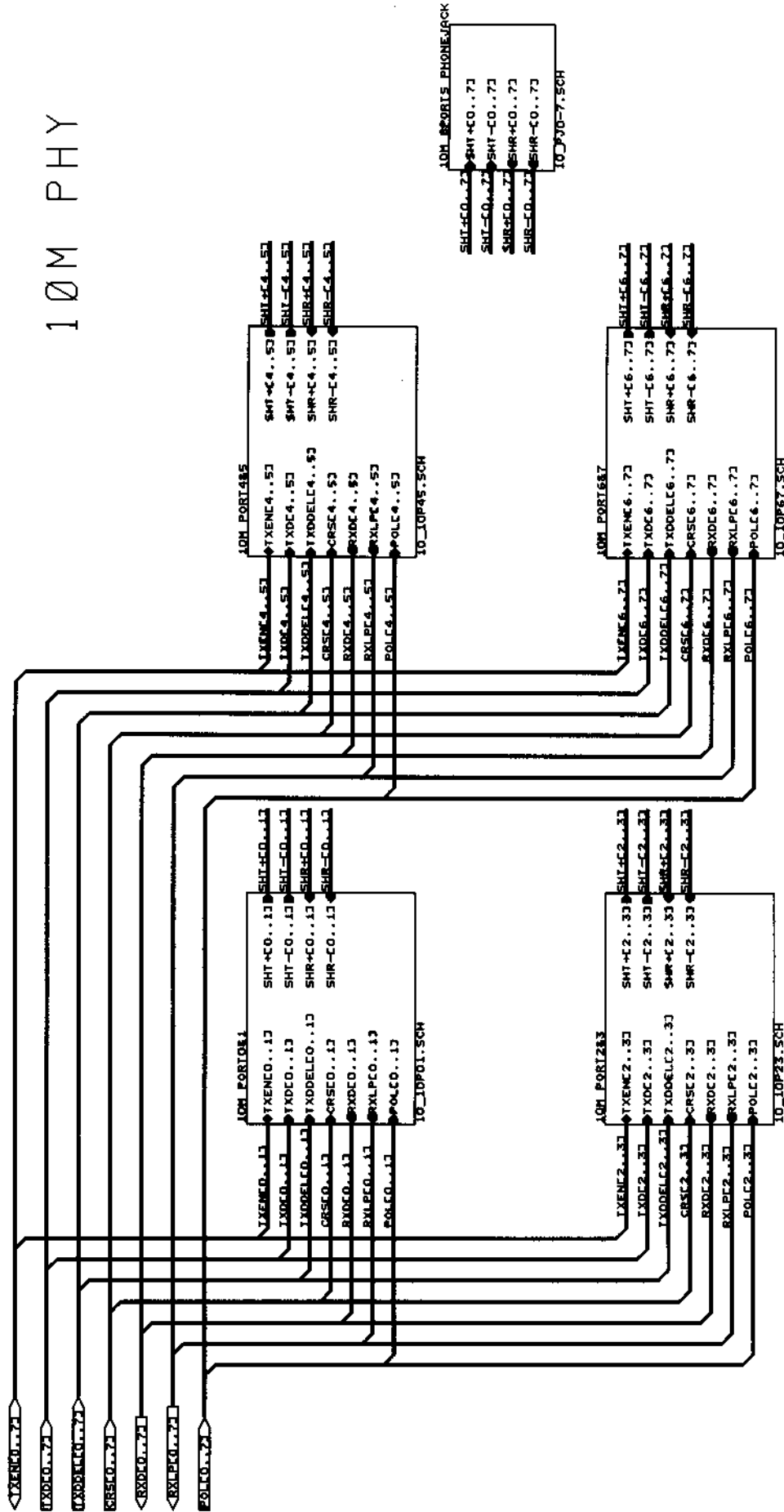
Version: A

DOC. NO.: 305DES810---A2-

Date: February 15, 1998

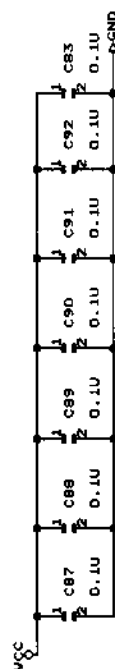
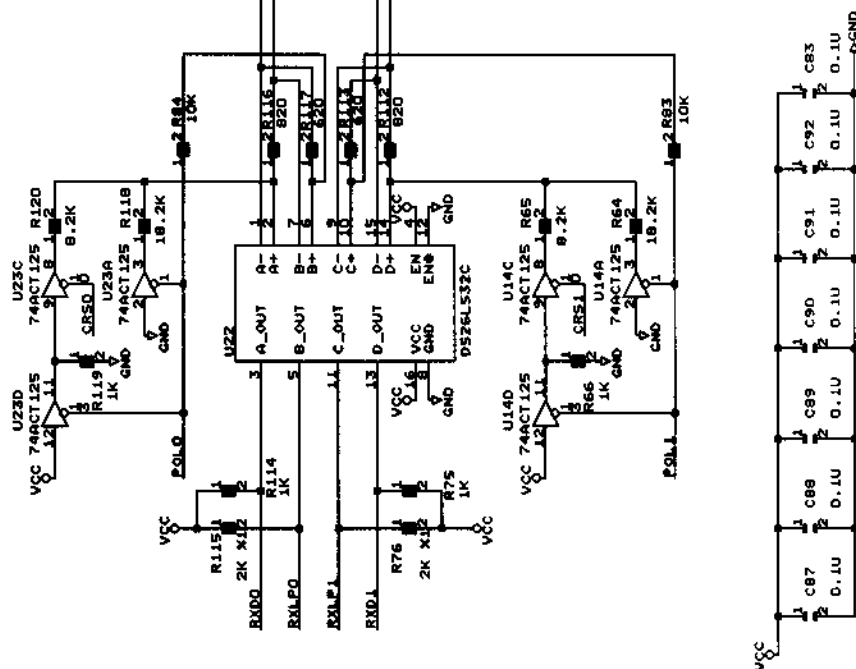
Sheet 3 of 21

10M PHY



10M PORT185
 TXNC4..53
 TXDC4..53
 TXDEL4..53
 CRSC4..53
 RXDC4..53
 RXLP4..53
 POLC4..53
 10M PORT187
 TXNC6..73
 TXDC6..73
 TXDEL6..73
 CRSC6..73
 RXDC6..73
 RXLP6..73
 POLC6..73
 10M PORT283
 TXNC2..33
 TXDC2..33
 TXDEL2..33
 CRSC2..33
 RXDC2..33
 RXLP2..33
 POLC2..33
 10M PORT687
 TXNC6..73
 TXDC6..73
 TXDEL6..73
 CRSC6..73
 RXDC6..73
 RXLP6..73
 POLC6..73
 10M PHY
 SHT-CO..73
 SHR-CO..73
 POLC..73
 10M PORT185
 SHT-CO..53
 SHR-CO..53
 POLC..53
 10M PORT187
 SHT-CO..73
 SHR-CO..73
 POLC..73
 10M PORT283
 SHT-CO..33
 SHR-CO..33
 POLC..33
 10M PORT687
 SHT-CO..73
 SHR-CO..73
 POLC..73

D-Link Corp.		Approved: <i>[Signature]</i>	Prepared: POLLY PAN
Doc. No.: 305DES810-...-A2-		Checked: <i>[Signature]</i>	Issued Date:
Version: A		Title: DES-810/DES-818's LOM_PCB	Size: 8
Date: February 16, 1998		Sheet: 4 of 21	REV: A2



D-Link

Approved: [Signature] Prepared: 7/2/00 : POLLY PAN

01/25/2010	Issued Date :
Checked by :	Title :

015-810-0E

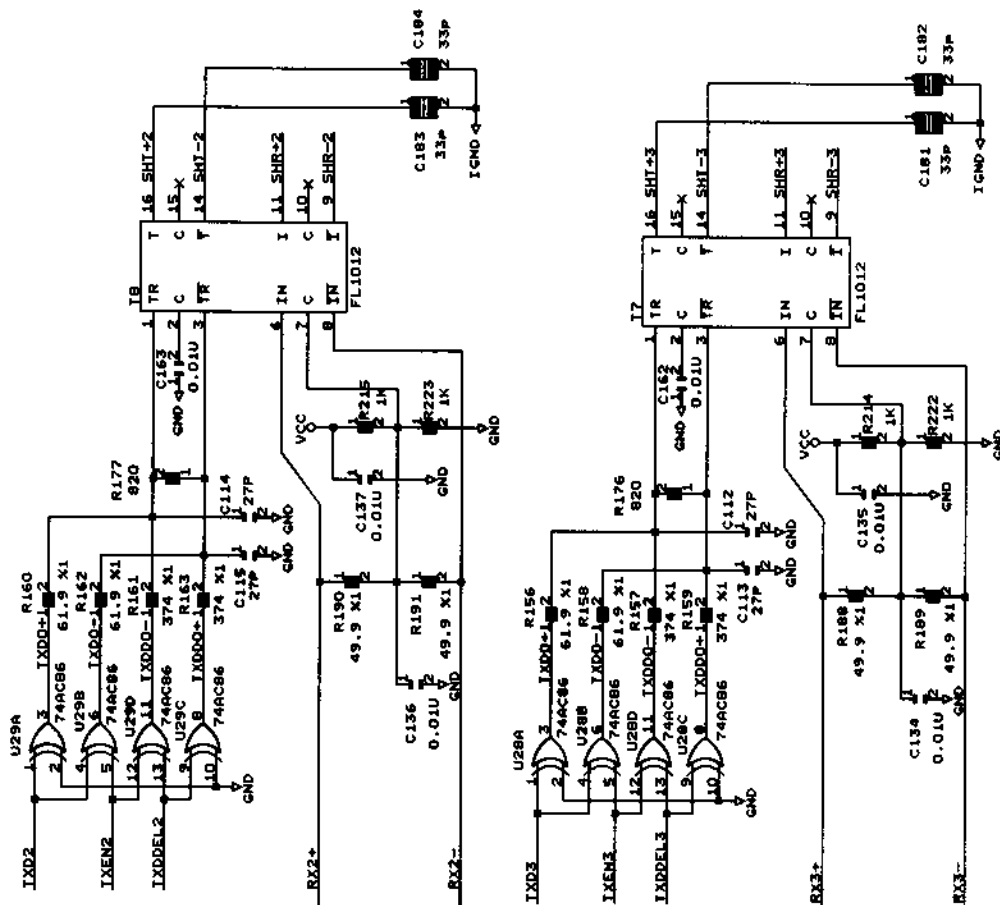
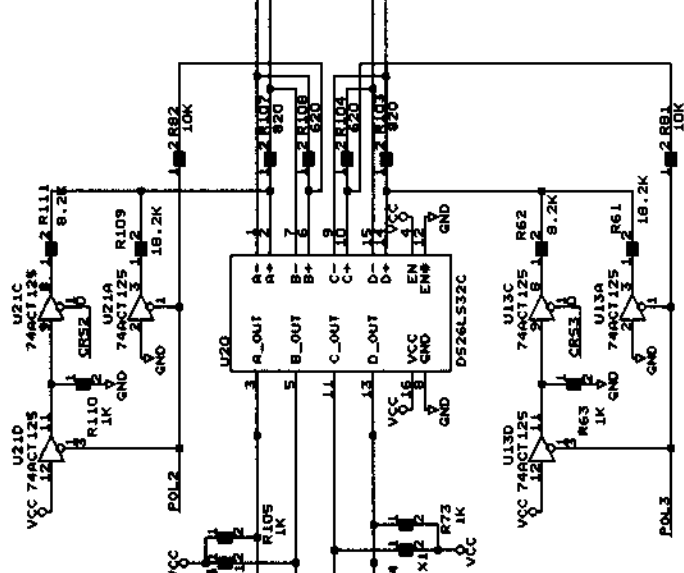
DOC. NO.: 305DES810-----A2-

Size	B	07A-00-0000-M30
Document Number		0EM-0000-00-V10

Date: February 16, 1998 Sheet 5

Date: February 16, 1998 Sheet 5

Date: February 16, 1998 Sheet 5



D-Link®

DOC. NO.: 305DEC010

Approved: [Signature] : POLLY PAN

Issued Date : 16/06/2018

Chickadee

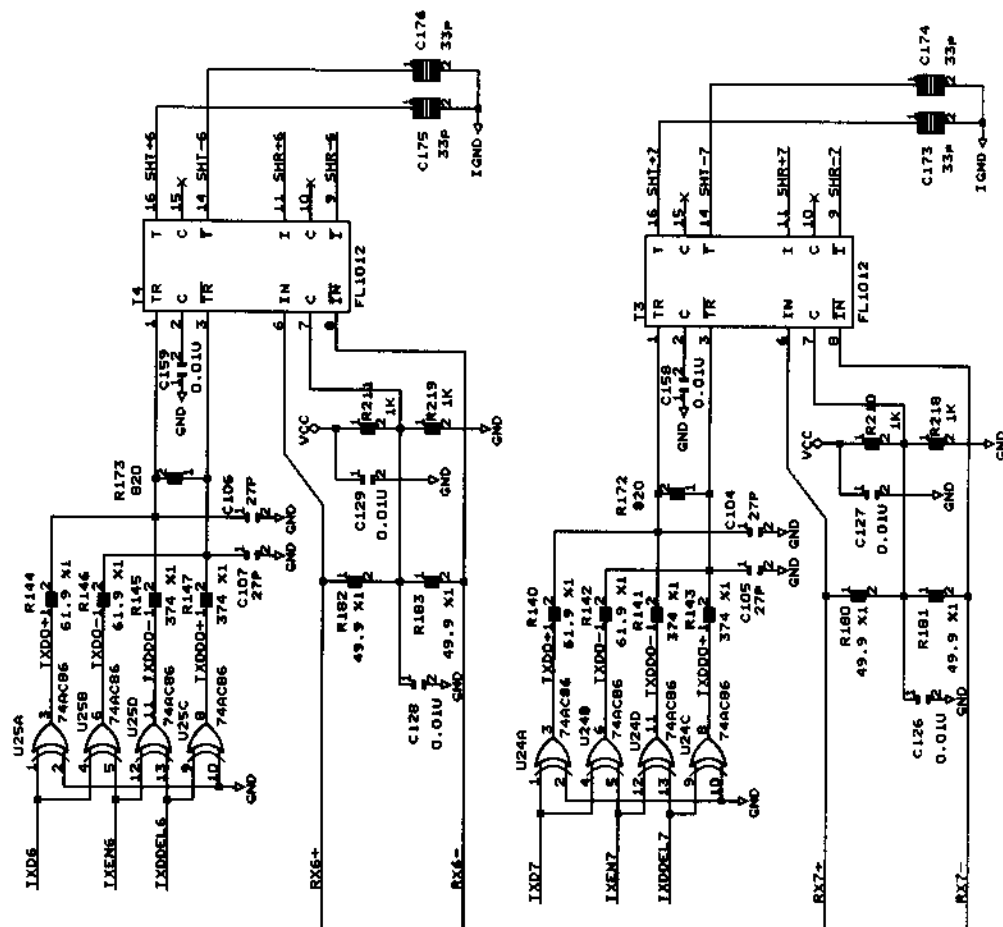
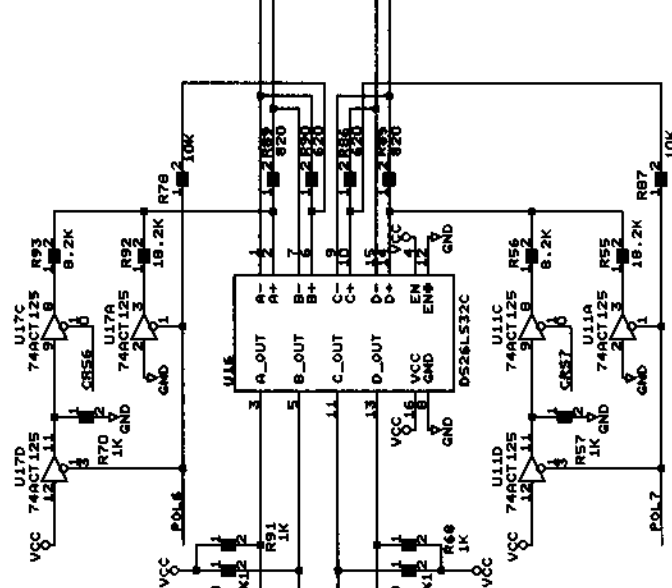
Version = 1

Size Document Number

QTA-00-0000-M30	8
-----------------	---

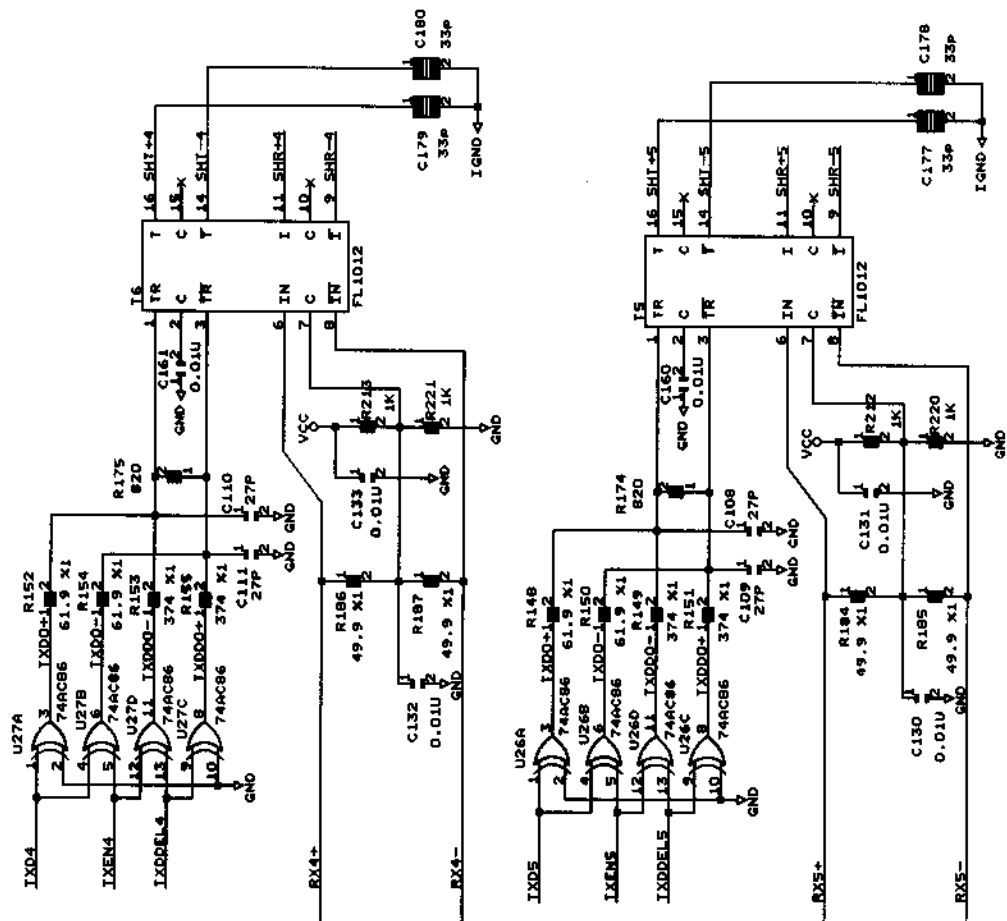
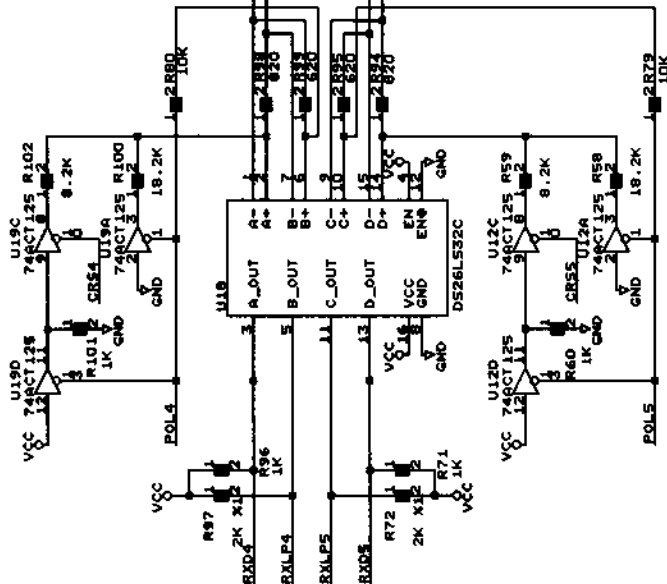
A2	
----	--

Figure 1: Schematic representation of the DNA constructs used in the study. The figure shows six DNA constructs: pSHT, pSHT-S, pSHR, pSHR-S, pSHT-S-S, and pSHR-S-S. Each construct is represented by a horizontal line with various elements labeled: 'ori' (origin of replication), 'SHT' or 'SHR' (structural genes), 'S' (signal sequence), and 'p' (promoter). The constructs are arranged in two rows of three. The top row shows pSHT, pSHT-S, and pSHR. The bottom row shows pSHR-S, pSHT-S-S, and pSHR-S-S. The constructs are labeled with their respective names and the number of base pairs (bp) for each segment.



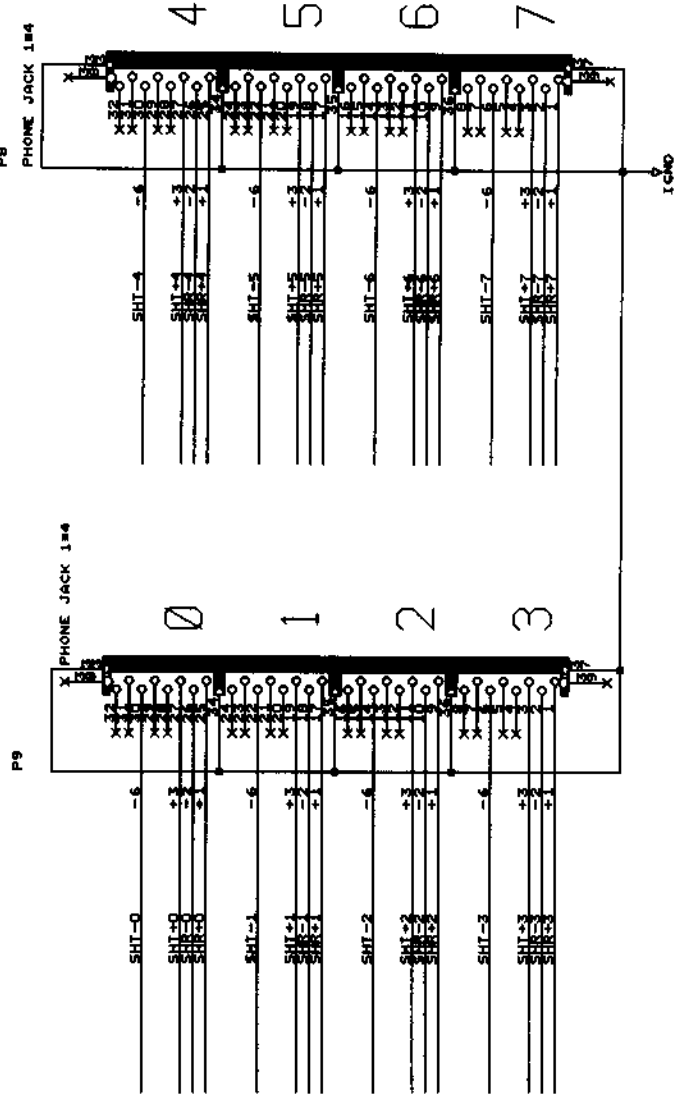
	Approved: <u>張福財</u> 1998 Checked: <u>張福財</u> 1998 Issued Date: _____		Prepared: _____ Title: _____ Issued Date: _____		PCC : POLLY PAN	
	Doc. No.: 305DES810- ---A2-		Size Document Number B OEM-0000-00-V10 Version: A		REV A2 Date: February 16, 1998 Sheet 7 of 21	

Figure 1 shows a schematic representation of the 12 genes of the 12S rDNA cluster. The genes are arranged in two rows. The top row contains genes 10, 11, 12, and 13. The bottom row contains genes 1, 2, 3, and 4. Each gene is represented by a horizontal bar with a central box and a tail. The central box contains the gene number and the number of repeats. The tail contains the repeat sequence. For example, gene 10 has 10 repeats of the sequence 5'-TGT-4...5'.



D-Link® Corp.		Approved:  Checked: 	Prepared:  Issued Date:	POLLY PAN
DOC. NO.: 305DES10- - - - A2-		Title: DES-810/DES-818's LOW_FCB		
Version: A		Size: Document Number		
Date: February 16, 1998		Date: February 16, 1998		
Sheet 8 of 21		REV A2		

SHT-C0...71
 SHT-C0...71
 SHT-C0...71
 SHT-C0...71

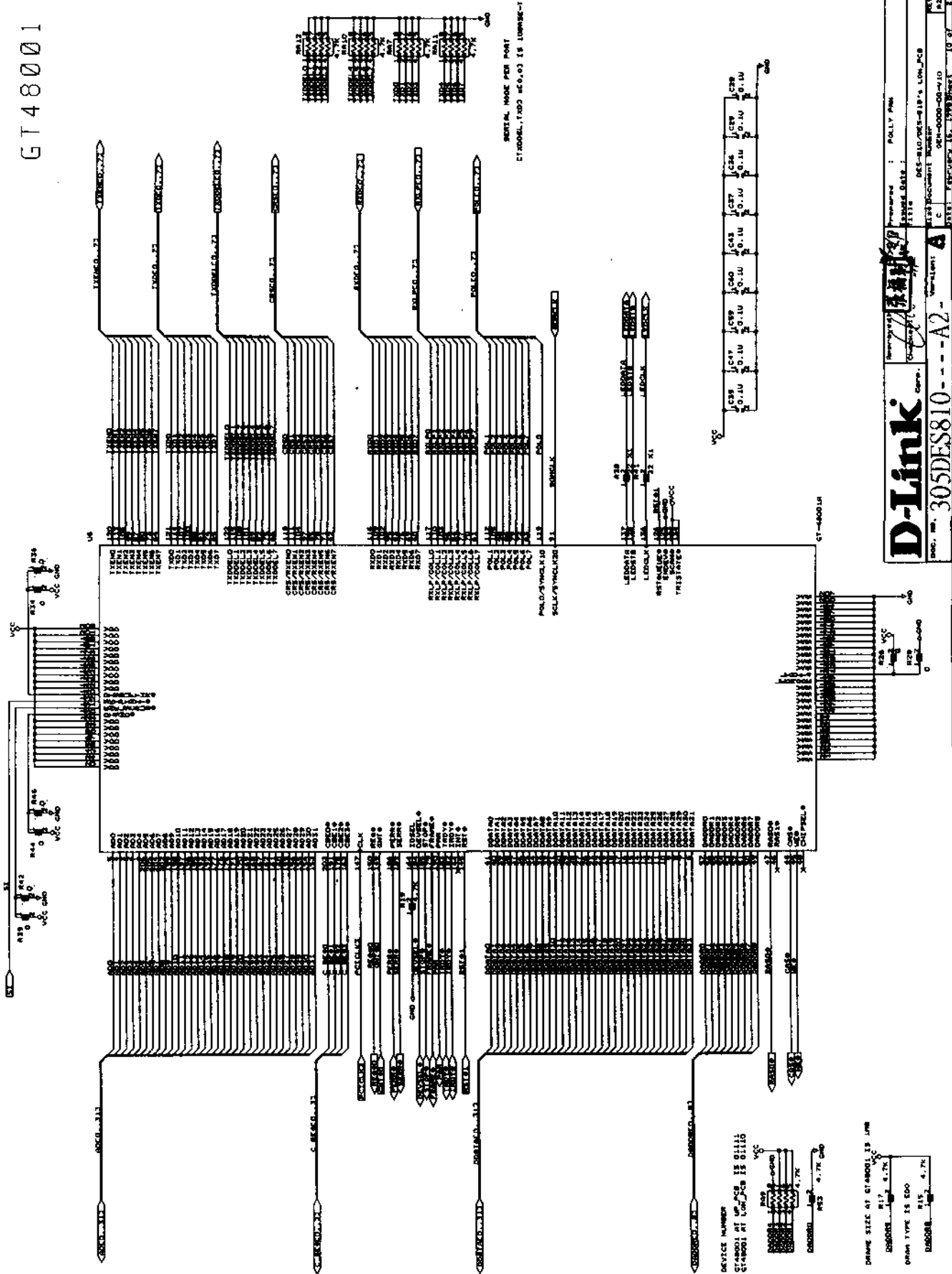


D-Link®

Approved: *[Signature]*
 Prepared: POLLY PAN
 Checked: *[Signature]*
 Issued Date: *[Date]*
 Title: DES-810/DES-818's LOM_PCB
 Size Document Number: B
 Version: A
 Date: February 15, 1998
 Sheet 9 of 21
 REV A2

DOC. NO.: 305DES810---A2-

GT48001



D-Link

305DES10 - A2

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

GT48001

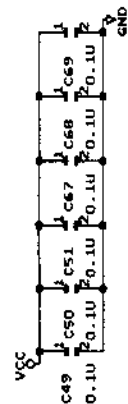
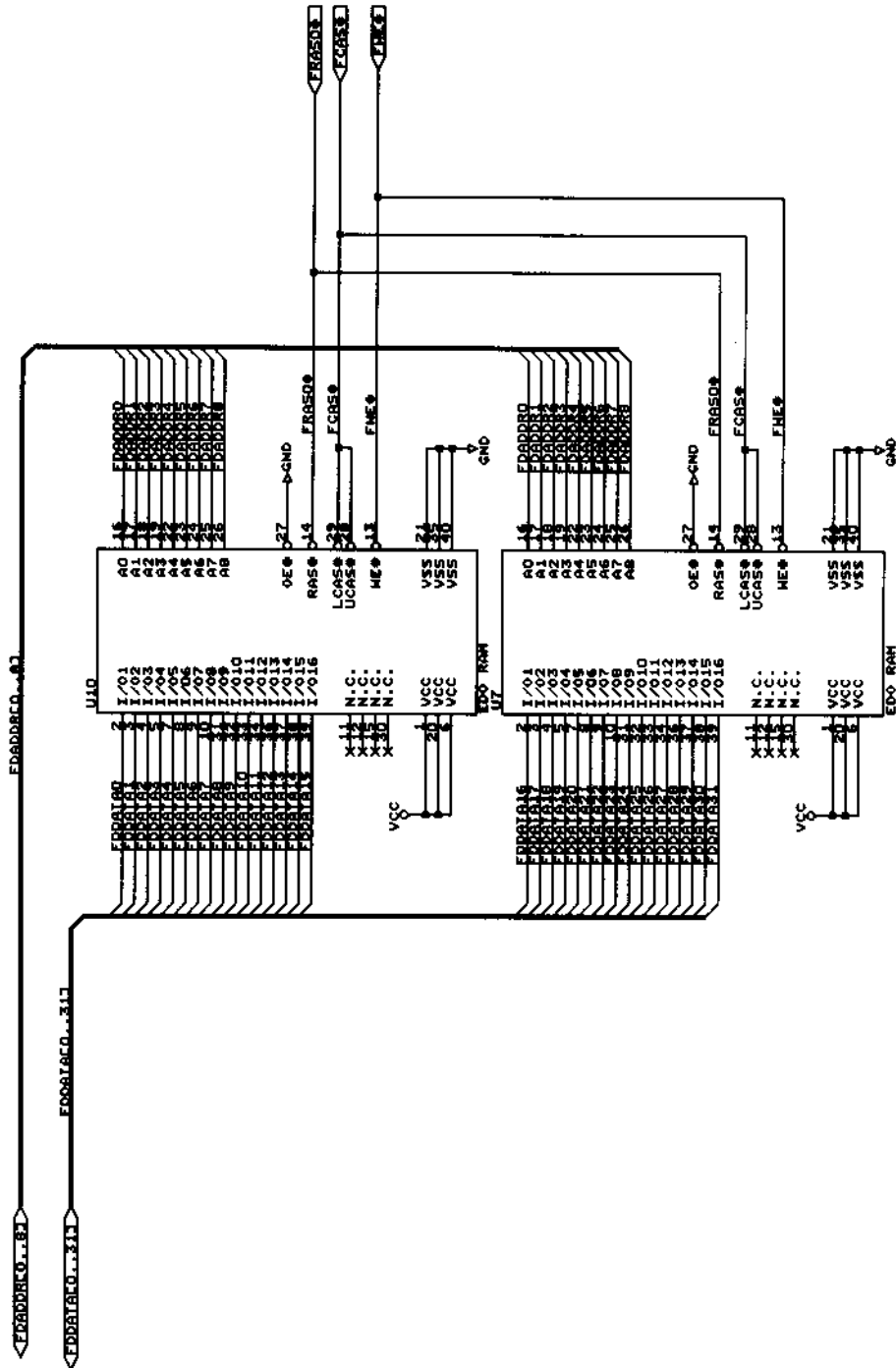
GT48001

GT48001

ROOM SWITCH CONTROLLER



DRAM FOR GT48002 IS 1MB



D-Link Corp.		Approved: <i>Chen</i> Checked: <i>Shih</i> Title: <i>210</i>	Prepared: POLLY PAN Issued Date:
Doc. No.: 305DES810--A2-	Version: A	Size: 110	Size: 110
Title: DES-810/DES-819's LOW PCB		Size: 110	Size: 110
Date: February 16, 1998		Date: February 16, 1998	Date: February 16, 1998
REV: 42		REV: 42	

PCB LAYOUT

CIRCUIT BOARD

4.7K

10K

100K

100N

VCC

GND

PCB LAYOUT

CIRCUIT BOARD

4.7K

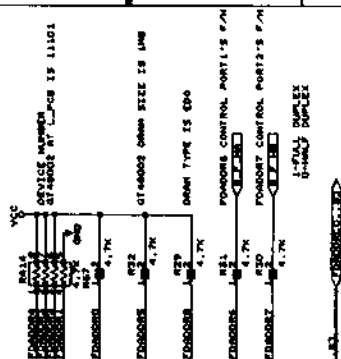
10K

100K

100N

VCC

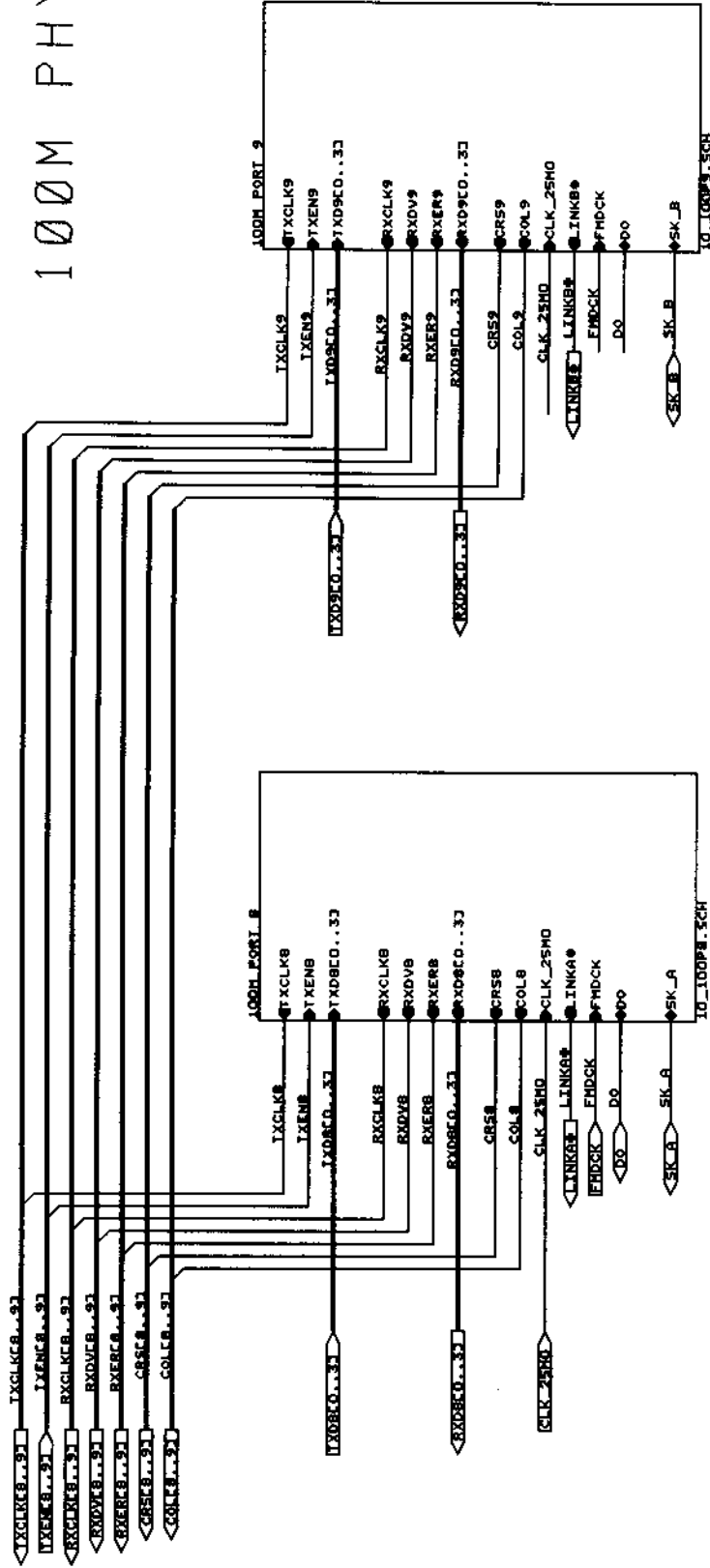
GND



D-Link

Doc. no.	305DES810	- - - A2 -	Version:	A
			ISS Document Number	C
				06M-0000-00-v10
				P2
				REV

100M PHY



D-Link
Corp.

DOC. NO.: 305DES810-...-A2-

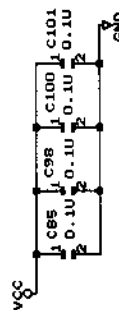
Approved: *[Signature]* 2/14/98
Checked: *[Signature]* 2/10/98
Title: DES-810/DES-818's LON_PCB

Version: A
Size Document Number: B
Date: February 16, 1998
REV A2 14 of 21


```

M16692 CAN CONFIG 3 MODES WHEN RESET
A:EDIN F100110;MUST BE ADD 93C44;
SEL0004 F000110;SEL 3445;PK (CONT)
SEL0004 F000110;SEL 3445;PK (CONT)
B:EDIN HIGH;LUSE LOGIC OR MICRO P;
SEL0004 F000110;SEL 3445;PK (CONT)
SEL0004 F000110;SEL 3445;PK (CONT)
C:EDIN LOW;
PL6692 DEFAULT VALUE
CHANGE SETTING BY MDC/MADIO

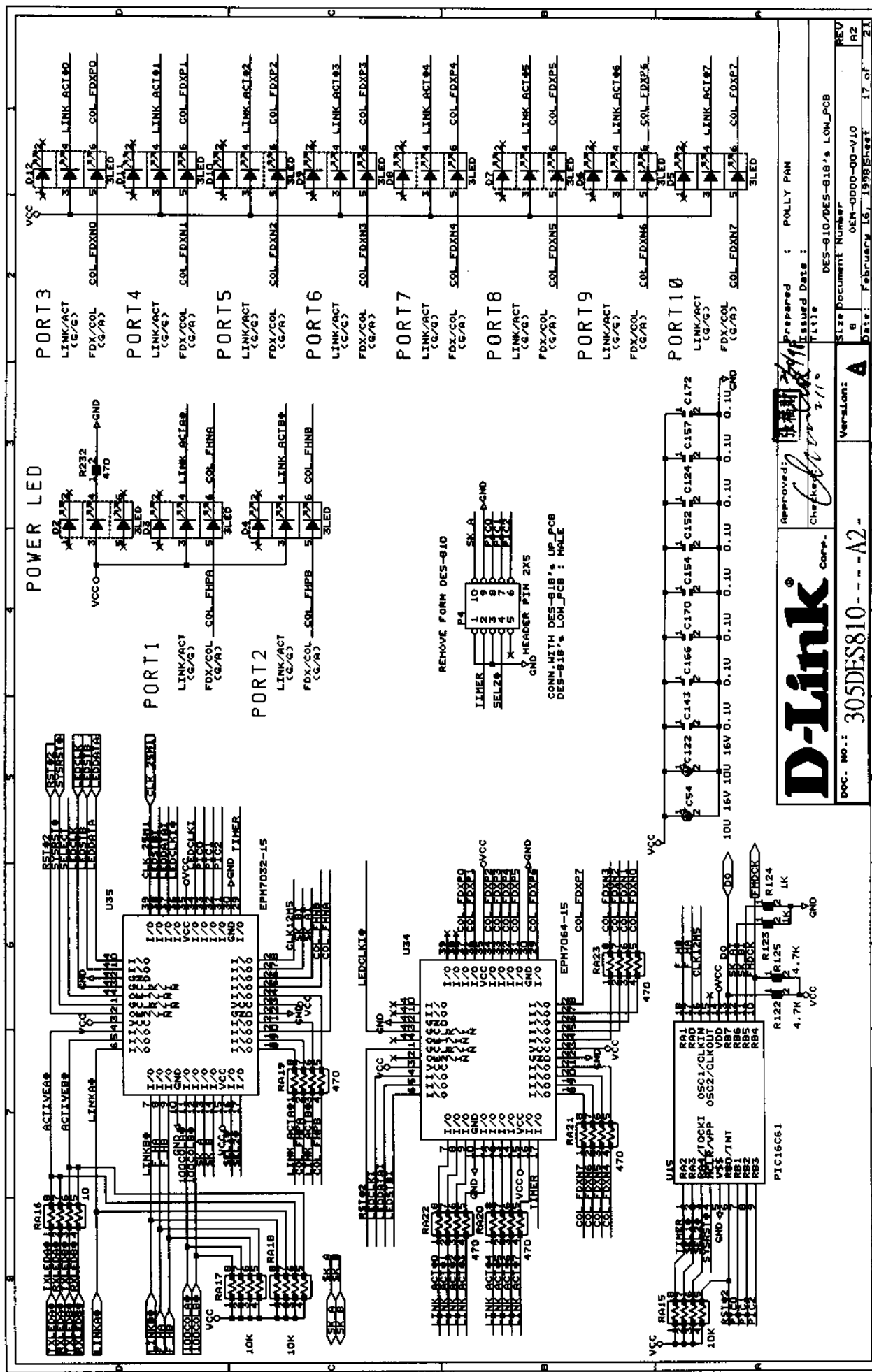
```



D-Link®

Approved: <u>張福蘭</u>	Prepared: <u>3/9/98</u>	POLLY PAN	
Checked: <u>何志強</u>	Issued Date: <u>3/10</u>	DES-810/DES-818's LON-PCB	
	Size: <u>21.0</u>	Version: <u>A</u>	Sheet 15
		Date: <u>February 16, 1998</u>	Sheet 15

DOC. NO.: 305DES810----A2-

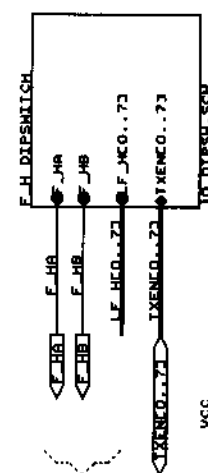
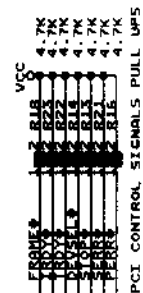


D-Link

Approved: *[Signature]*
Checked: *[Signature]*
Title: DES-810/DES-818's LON_PCB
Size Document Number: 8
Version: A
Date: February 16, 1995

DOC. NO.: 305DES810 --- A2 -
REV A2
REV 21

REMOVE FROM DES-810



FOR LED'S 7032

10-DIGSM-SCN

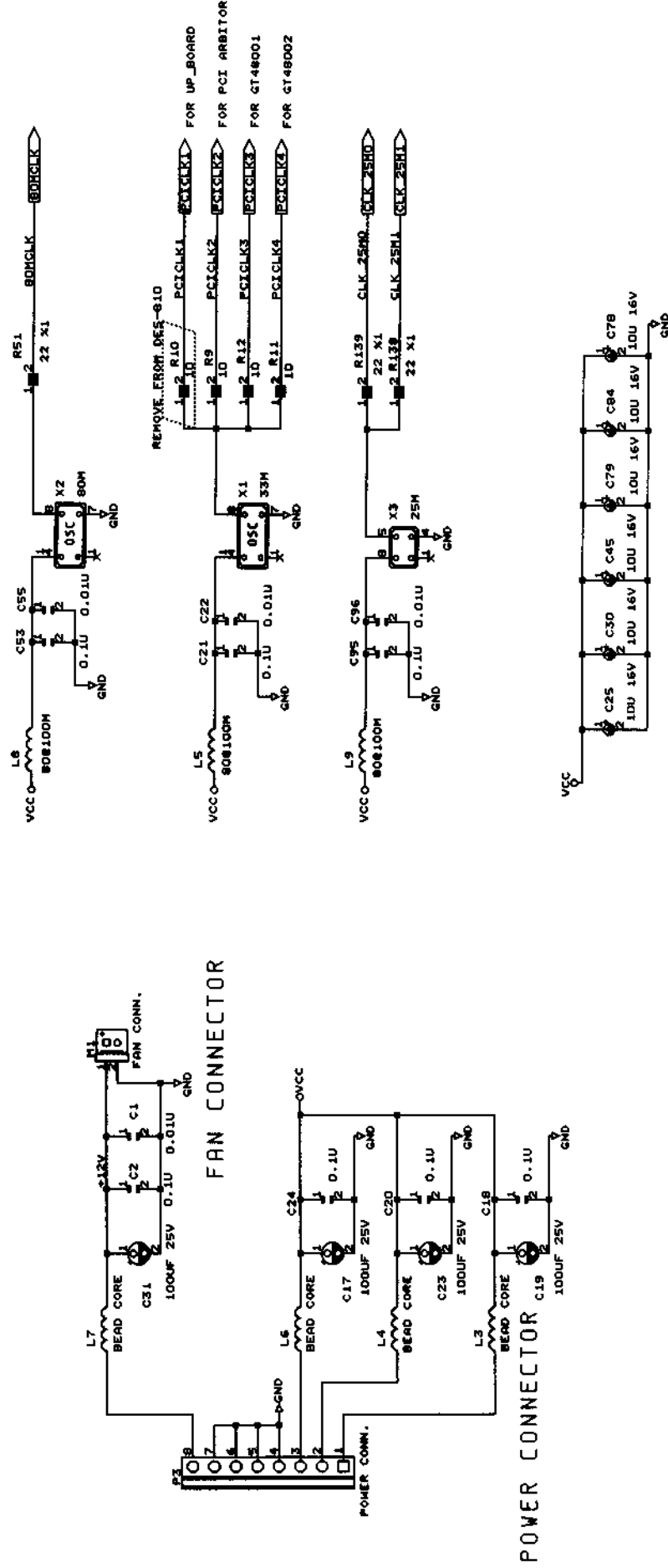
D-Link

: POLLY PAN

DOC. NO.: 305DES810-----A2--

Size	B	Document Number	OEM-0000-QD-V10	REV	A2
Date:	February 16, 1998	Sheet	18 of	21	

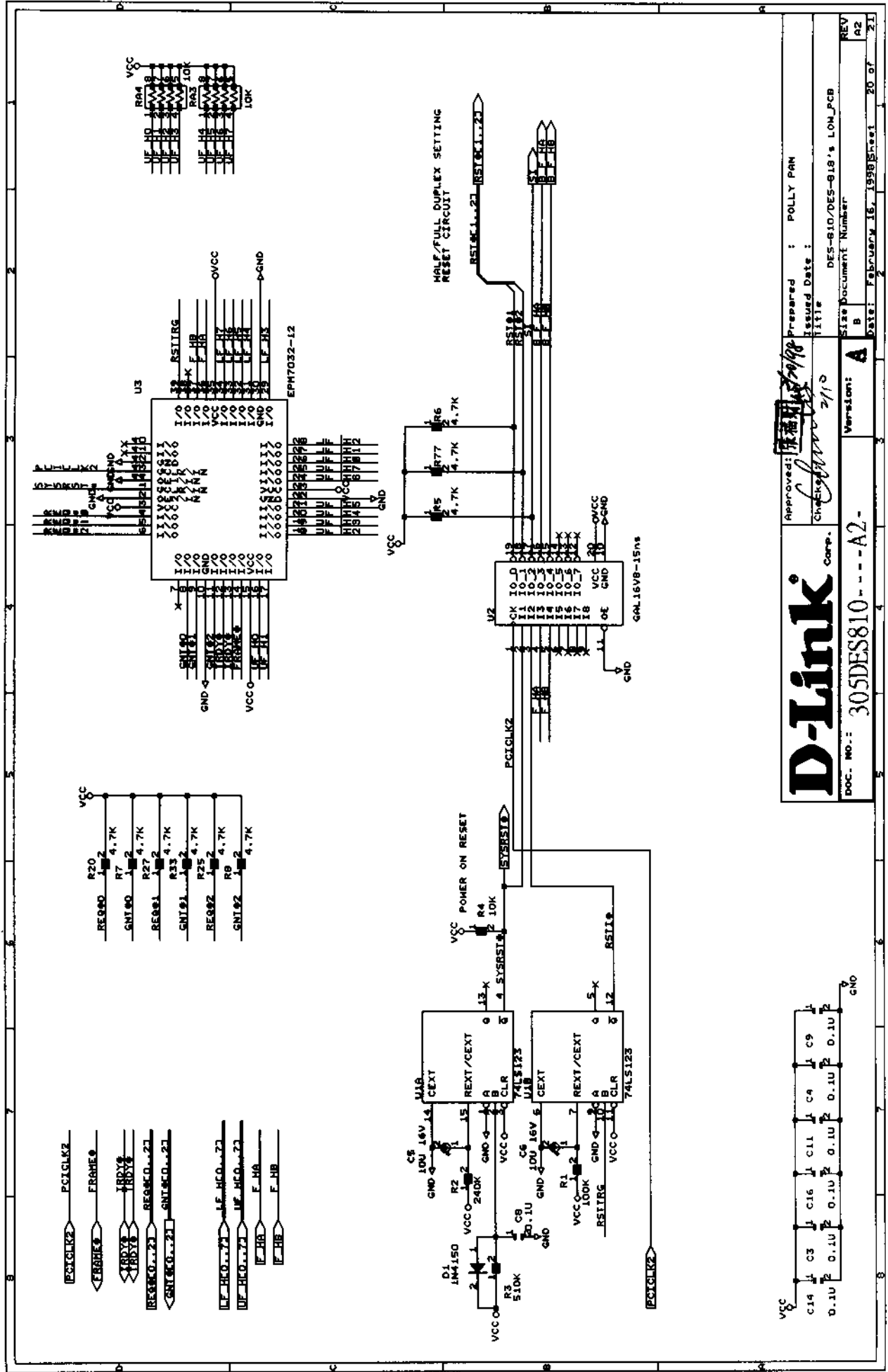
POWER AND CLOCK GENERATOR



D-Link

Doc. No.: 305DES810---A2-

Approved: *[Signature]* Prepared: POLLY PAN
 Checked: *[Signature]* Issued Date:
 Title: DES-810/DES-818's LON_PCB
 Size: Document Number
 Version: A
 Date: February 16, 1998 Sheet 19 of 21



D-Link Corp.		Approved: <i>[Signature]</i> Issued Date: 2/10/98 Title: DES-810/DES-818's LOW PCB	Prepared: POLLY PAN Size: B Date: February 16, 1998
DOC. NO.: 305DES810---A2-		Version: A	Sheet 20 of 21

