


生效日期: 87. 3. 17

DES 810 Rev. A1 電話図

REVISION	STATUS
0 ~ 0-1	A
1 ~ 21	A
	

APPROVED	CHECKED	DEPARTMENT	PREPARED
38 福慧林	X	卓裕文	Polly Ho

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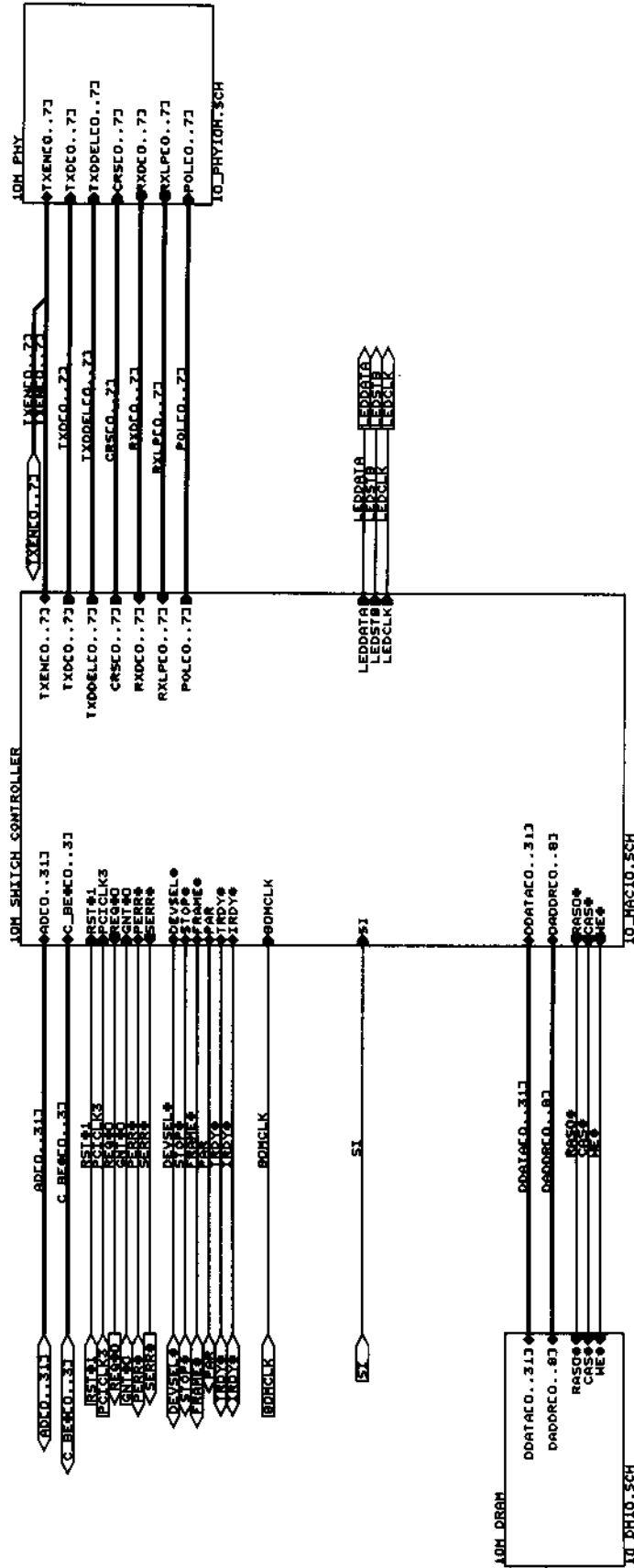
DOC. NO.: 305DES810-...A1-

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118-530/018-530	Title
Issued Date :	
Prepared : POLLY PAN	

Size	Document Number	REV
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Date	March 5, 1987	Sheet
		of 21

# 10M MAC CONTROLLER

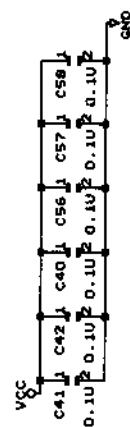


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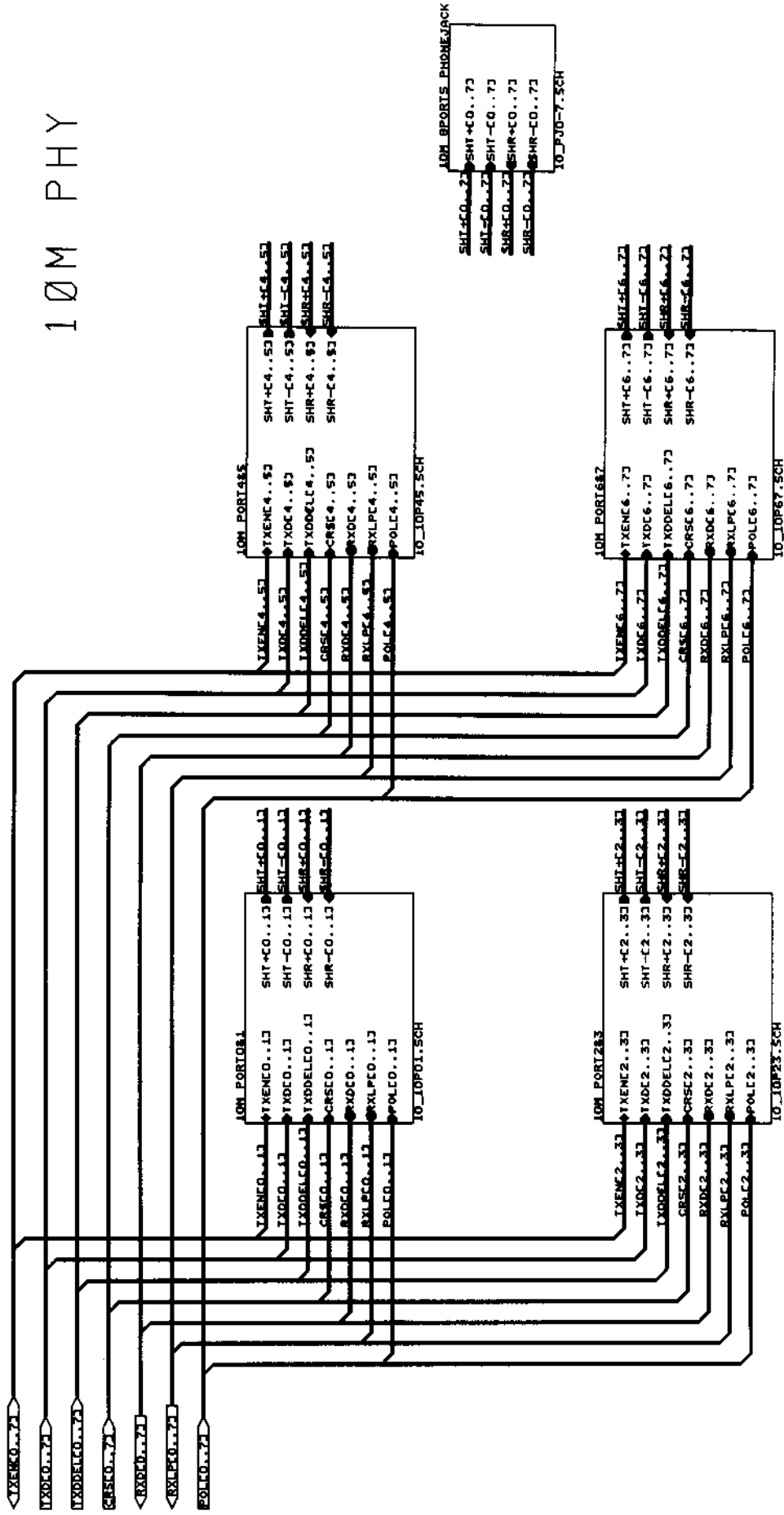
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DOC. NO.: 305DES810-000-A1-	Version: A	Size Document Number: B	REV: A1
Date: March 5, 1997		Sheet 2 of 21	



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10M PHY



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Title: DES-810/DES-818's 10M\_PCB

Size Document Number: DES-810/DES-818's 10M\_PCB

Rev: DES-810/DES-818's 10M\_PCB

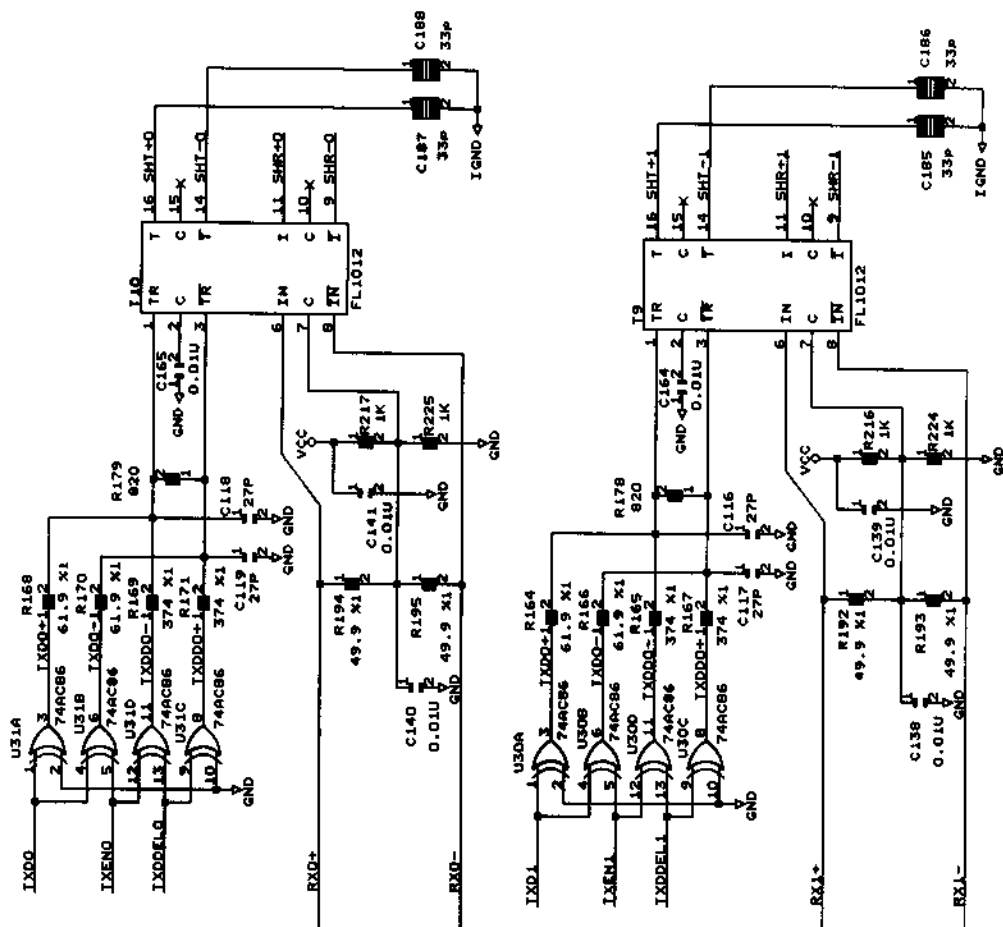
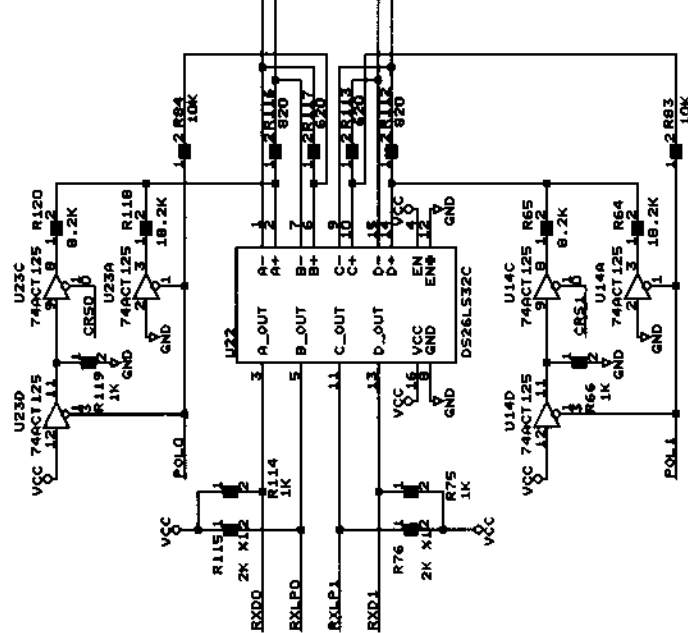
Date: March 5, 1997 Sheet 4 of 21

Doc. No.: 305DES810-1-A1

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**Appendix:**

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DOC. NO.: 305DES810-...-A1

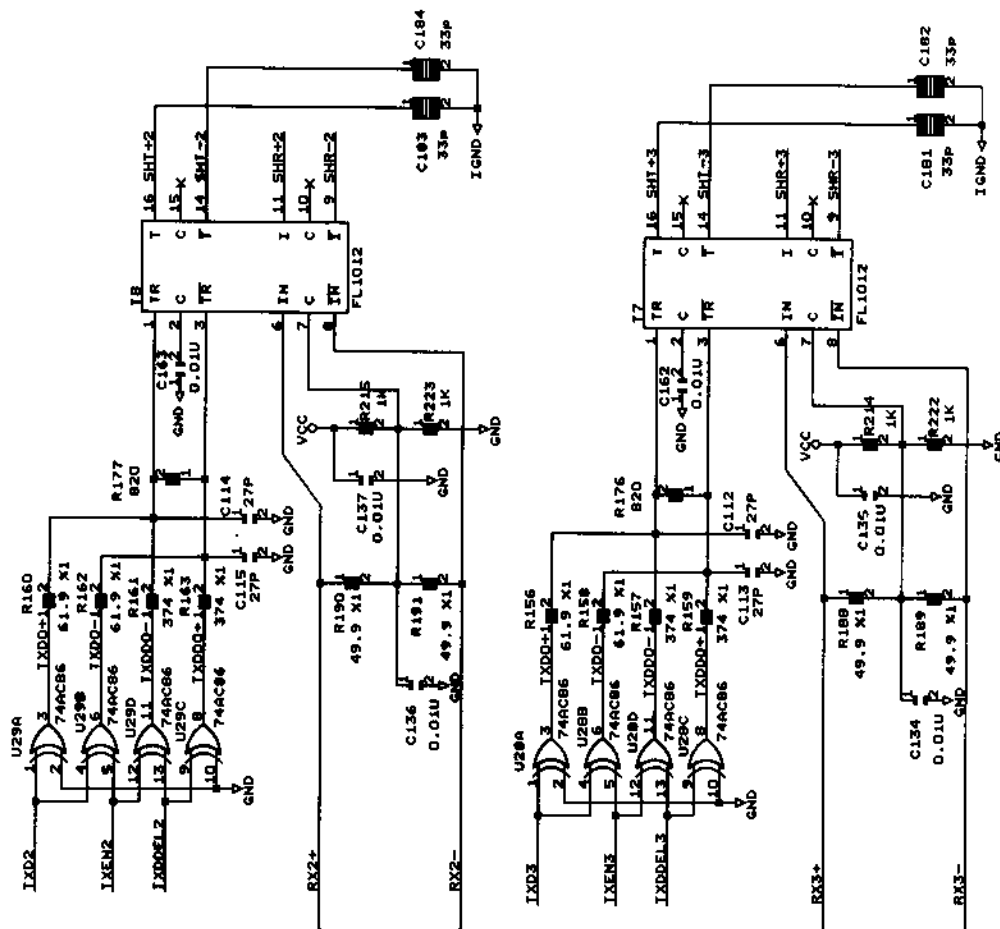
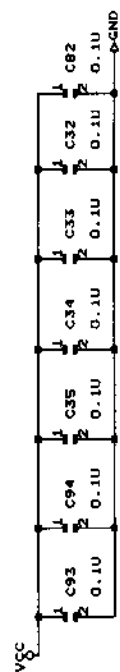
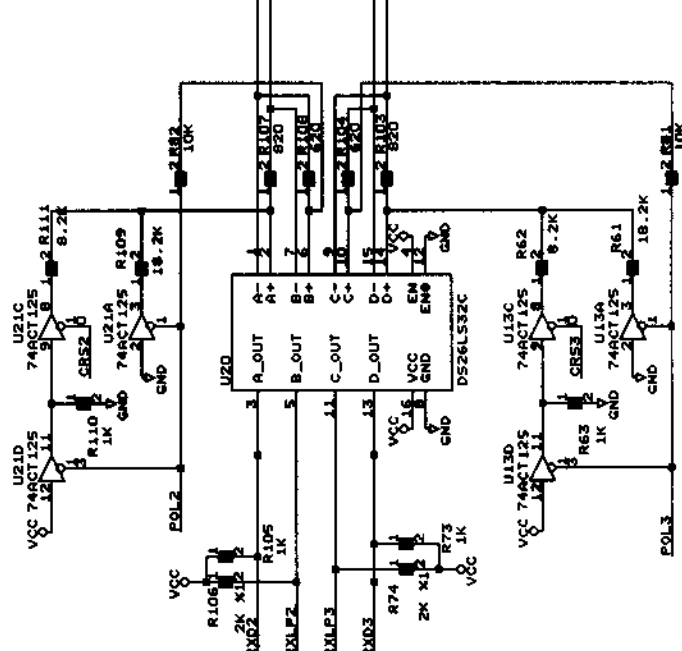
62-1107-9 070-270 (070-220)

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DTA=DD-DDDD=MAA

Date: June 10, 1997 Sheet 5

Figure 1: Schematic representation of the DNA constructs used in this study. The figure shows two sets of constructs. The left set includes LNC2-37, LNC2-37, LNC2-37, and LNC2-37. The right set includes LNC2-37, LNC2-37, LNC2-37, and LNC2-37. Each construct is represented by a horizontal line with a double arrow at the right end, indicating the direction of transcription. The constructs are labeled with their respective names and the number of nucleotides (nt) in parentheses.



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REPORT NUMBER 62-10700-1

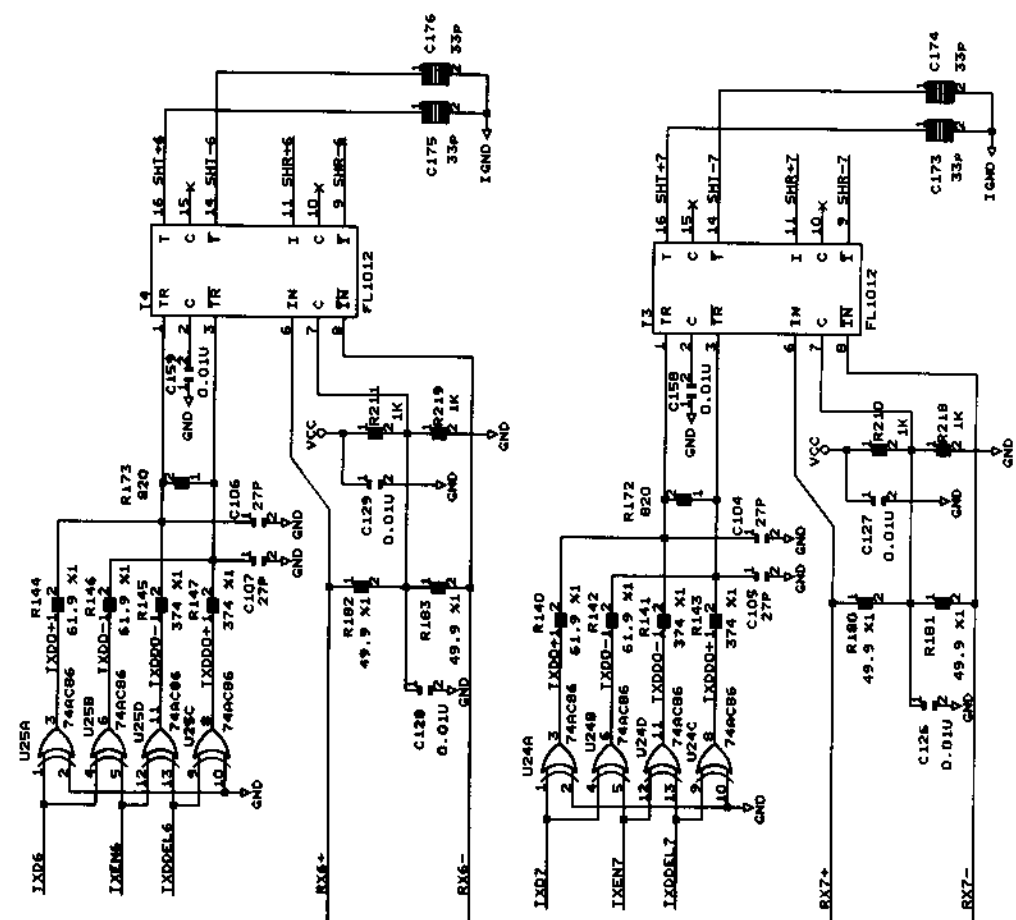
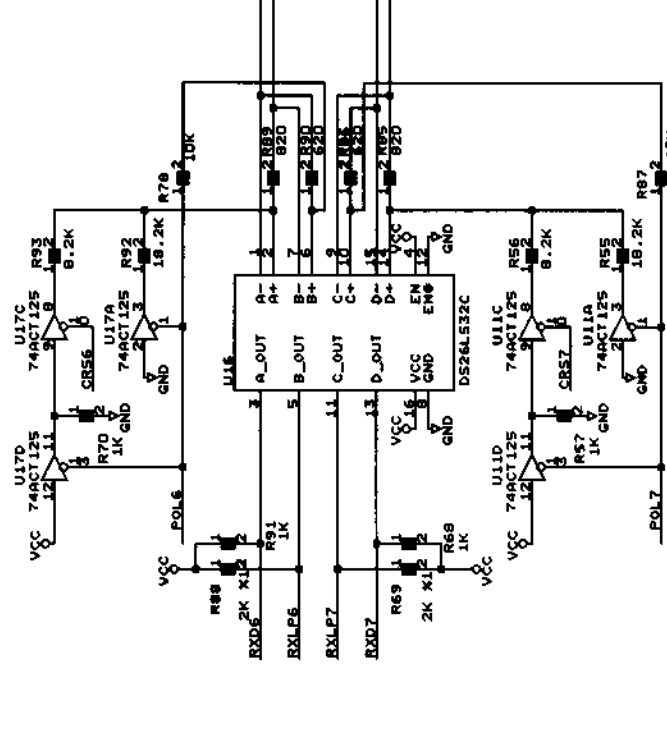
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Date: MAY 12, 1997 Sheet 6

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Figure 1 shows the schematic representation of the 12S and 12L protein structures. The 12S structure is composed of three subunits: one large subunit (L) and two small subunits (S). The 12L structure is composed of three large subunits (L). Each subunit is represented by a vertical bar with a series of dots indicating the amino acid sequence. The 12S structure is labeled '12S' and the 12L structure is labeled '12L'.



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DOC. NO.: 305DES810- - - - A1 -		Version: A		Size Document Number: 0ES-810/DES-810's LOW_PCB B Date: May 12, 1997 Sheet 7 of 21	

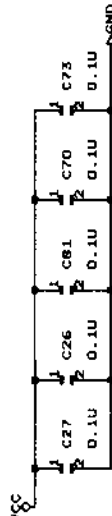
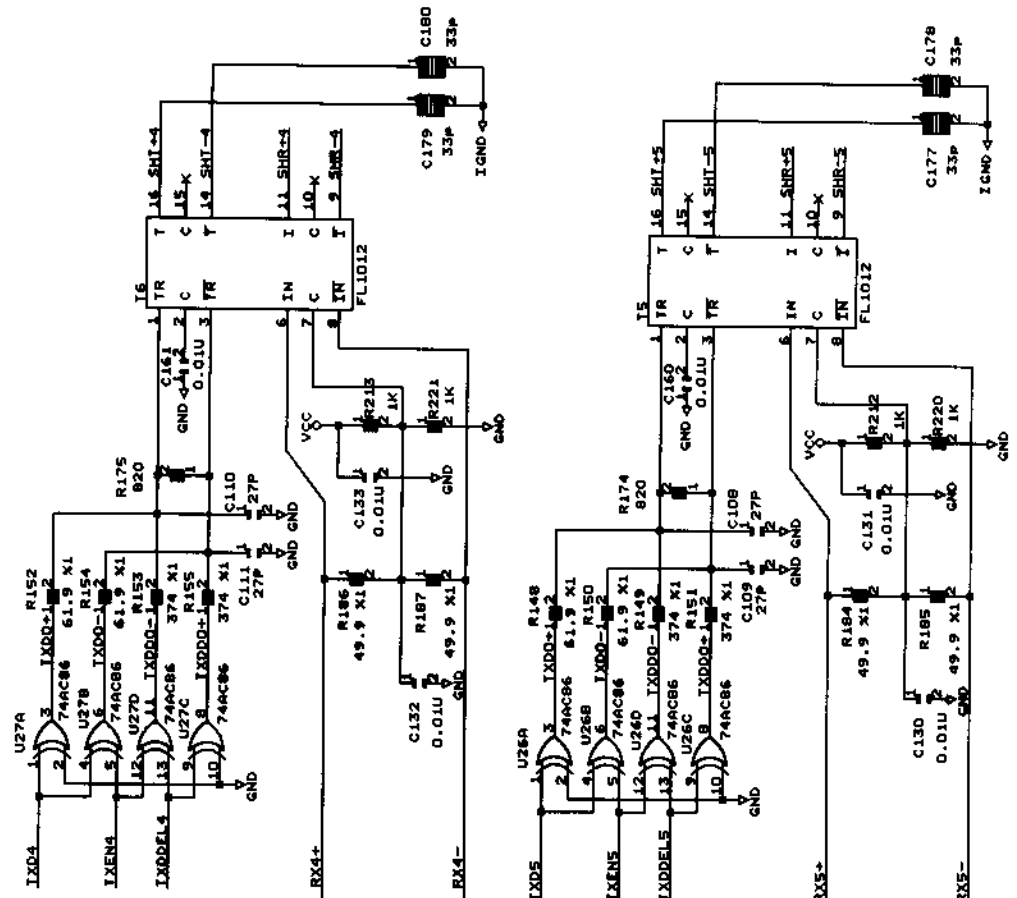
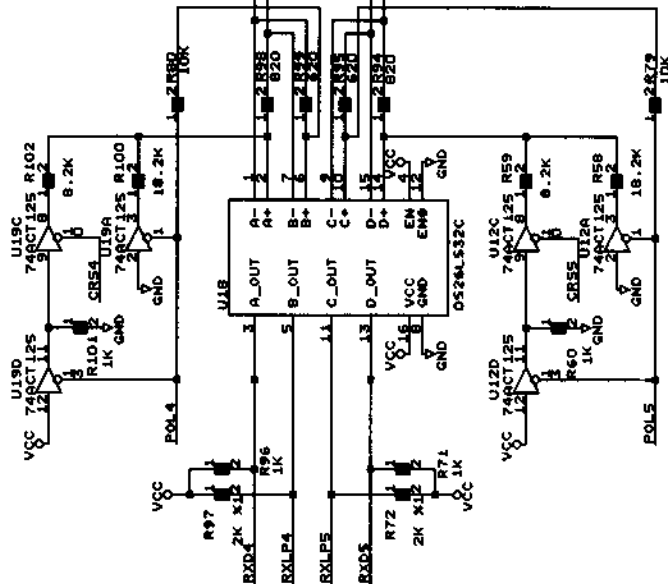

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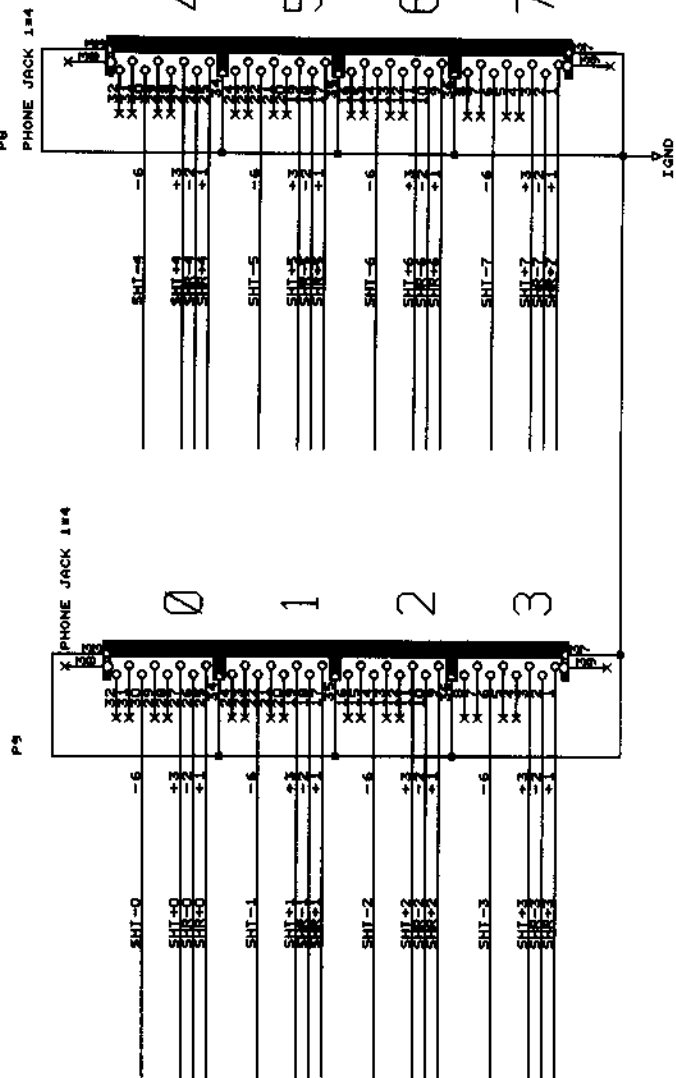
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# 10M PHY PORT4-5



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Doc. No.: 305DES810-A1-		Checked: <i>[Signature]</i>		Issued Date: _____	
Version: A		Title: DES-810/DES-818's LOM_PCB		Size Document Number: _____	
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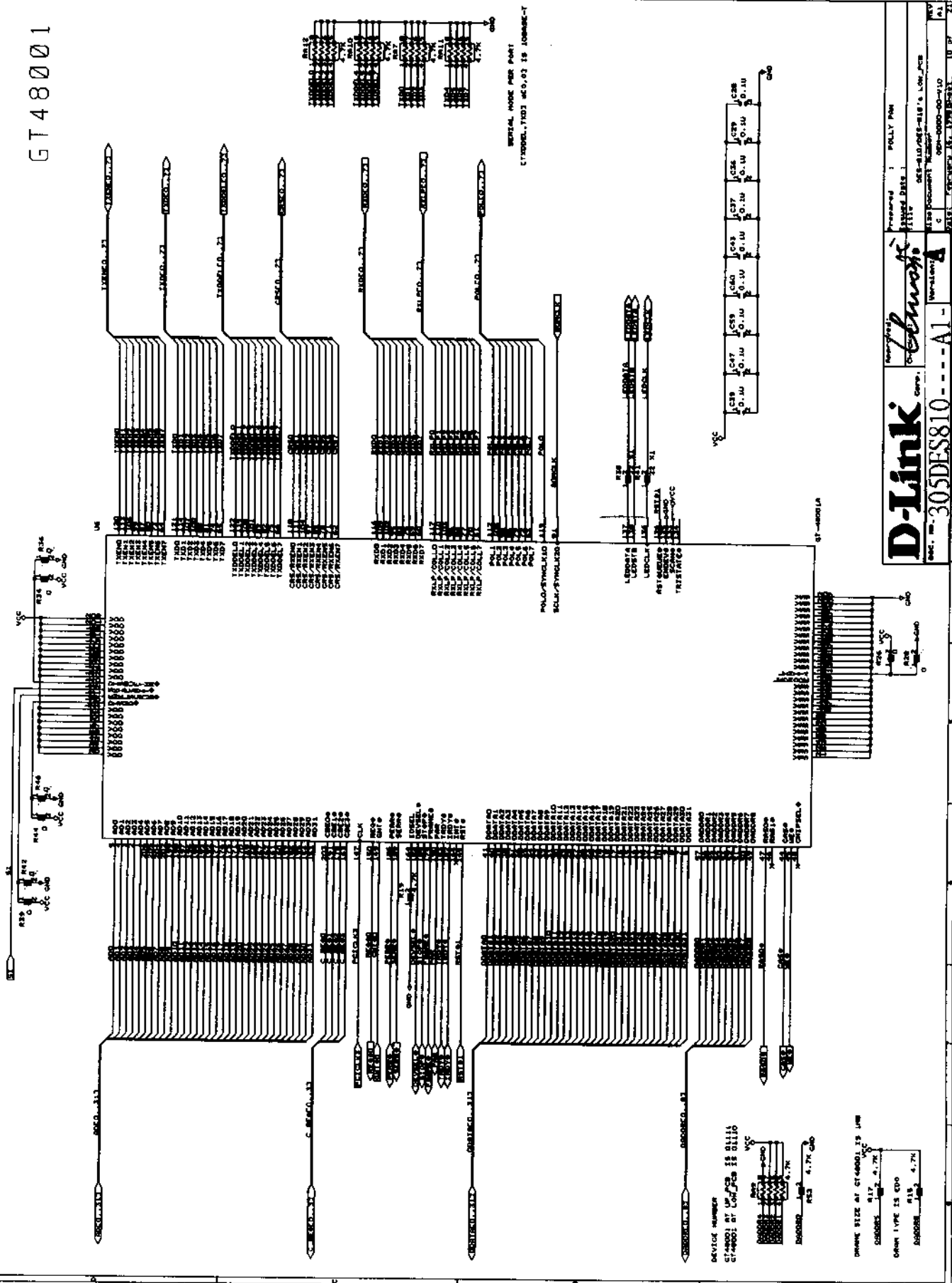
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Size Document Number

OEM-0008-PA-V11

Date: March 5, 1997 Sheet 3 of 21

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Part: 305DES810-A1 -

Rev: 1.0

DATE: 10/27/01

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Doc: 305DES810-A1 -

Rev: 1.0

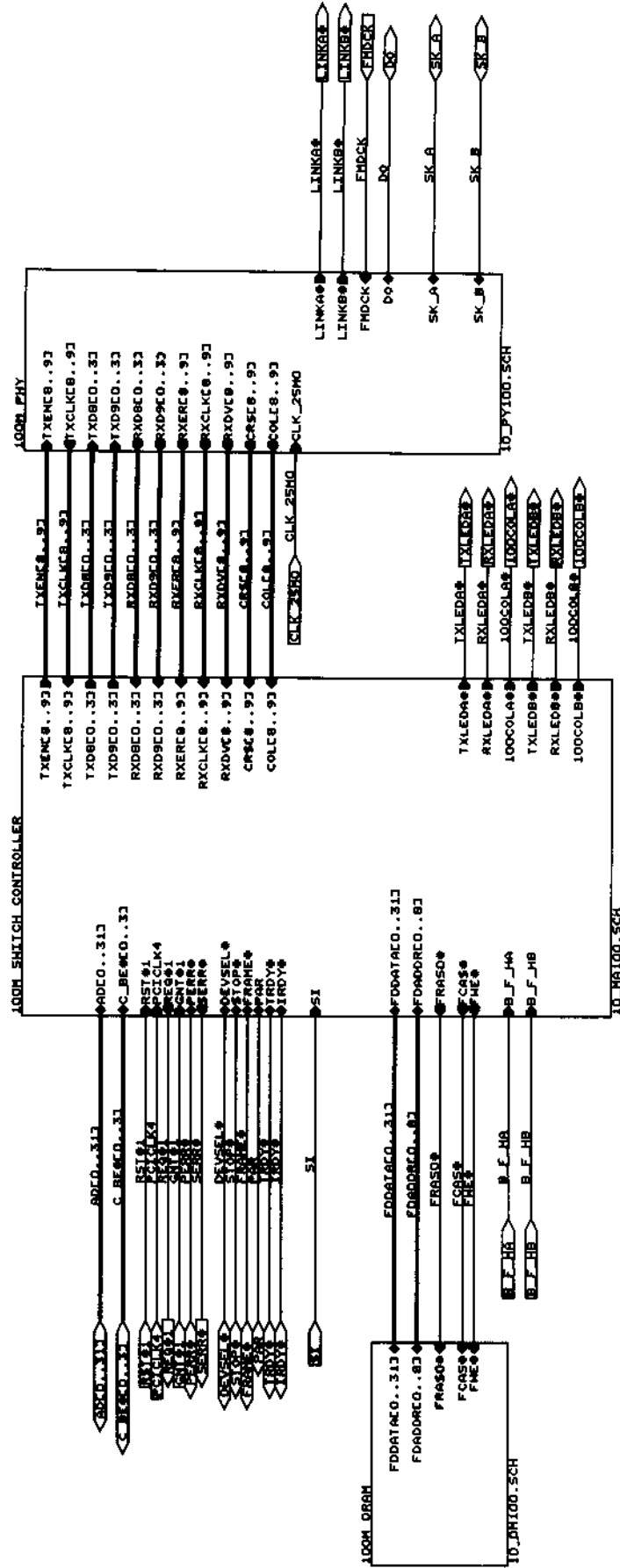
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Prepared: 1. POLLY PAM

Checked: 1. POLLY PAM

Approved: 1. POLLY PAM

# 100M MAC CONTROLLER



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DOC. NO.: 305DES810-1-A1-

Approved: *[Signature]*  
 Prepared: POLLY PAN  
 Revised Date: *[Date]*  
 Title: DES-810/DES-810's LON\_PCB  
 Size: Document Number  
 Version: A  
 Date: March 5, 1997 Sheet 11 of 21

The diagram illustrates the memory architecture for the TMS320C25, featuring two 16Kx16 RAM chips (U10 and U17) connected to a 32-bit data bus and a 16-bit address bus. The chips are organized into two banks, each containing 16K words of 16-bit data.

**Chip U10 (Left Bank):**

- Data Bus:** D[31:0] (pins 1-32).
- Address Bus:** A[15:0] (pins 16-31).
- Control Signals:** OE (pin 27), RAS (pin 14), CAS (pin 29), WE (pin 13), FCS (pin 28), FHE (pin 12).
- Power:** VCC (pins 1, 20, 30), VSS (pins 2, 21, 22, 31).

**Chip U17 (Right Bank):**

- Data Bus:** D[31:0] (pins 1-32).
- Address Bus:** A[15:0] (pins 16-31).
- Control Signals:** OE (pin 27), RAS (pin 14), CAS (pin 29), WE (pin 13), FCS (pin 28), FHE (pin 12).
- Power:** VCC (pins 1, 20, 30), VSS (pins 2, 21, 22, 31).

The diagram shows the internal structure of the RAM chips, including the data bus, address bus, and control signals. The chips are connected to the system bus via their respective pins, and the power supply is connected to the VCC and VSS pins.

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		DES-810/DES-818's LOW PCB	
DOC. NO.:	305DES810----	A1-	
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		Date:	March 19, 1997
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Prepared : POLLY PAN

**Issued Date :**

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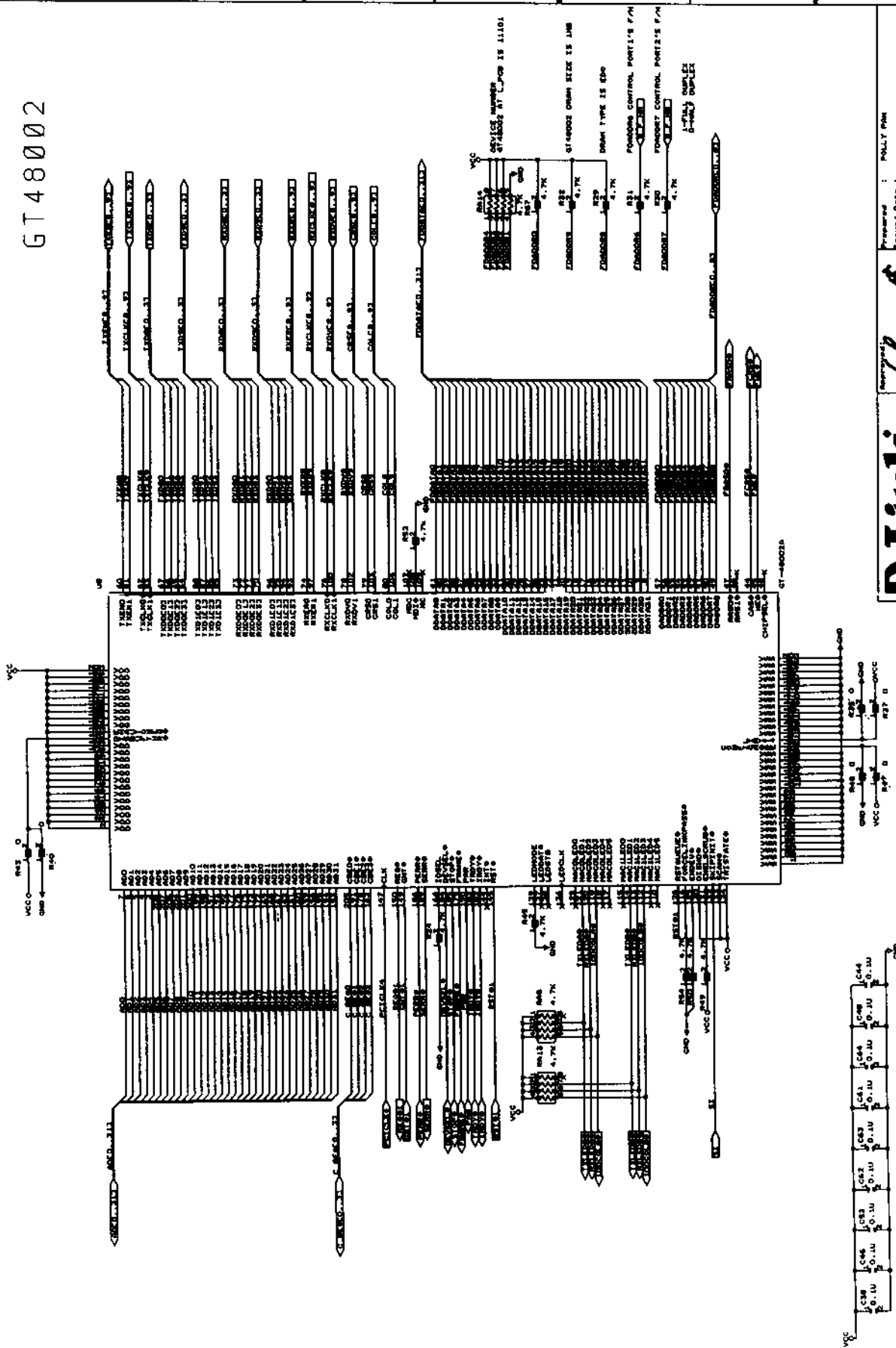
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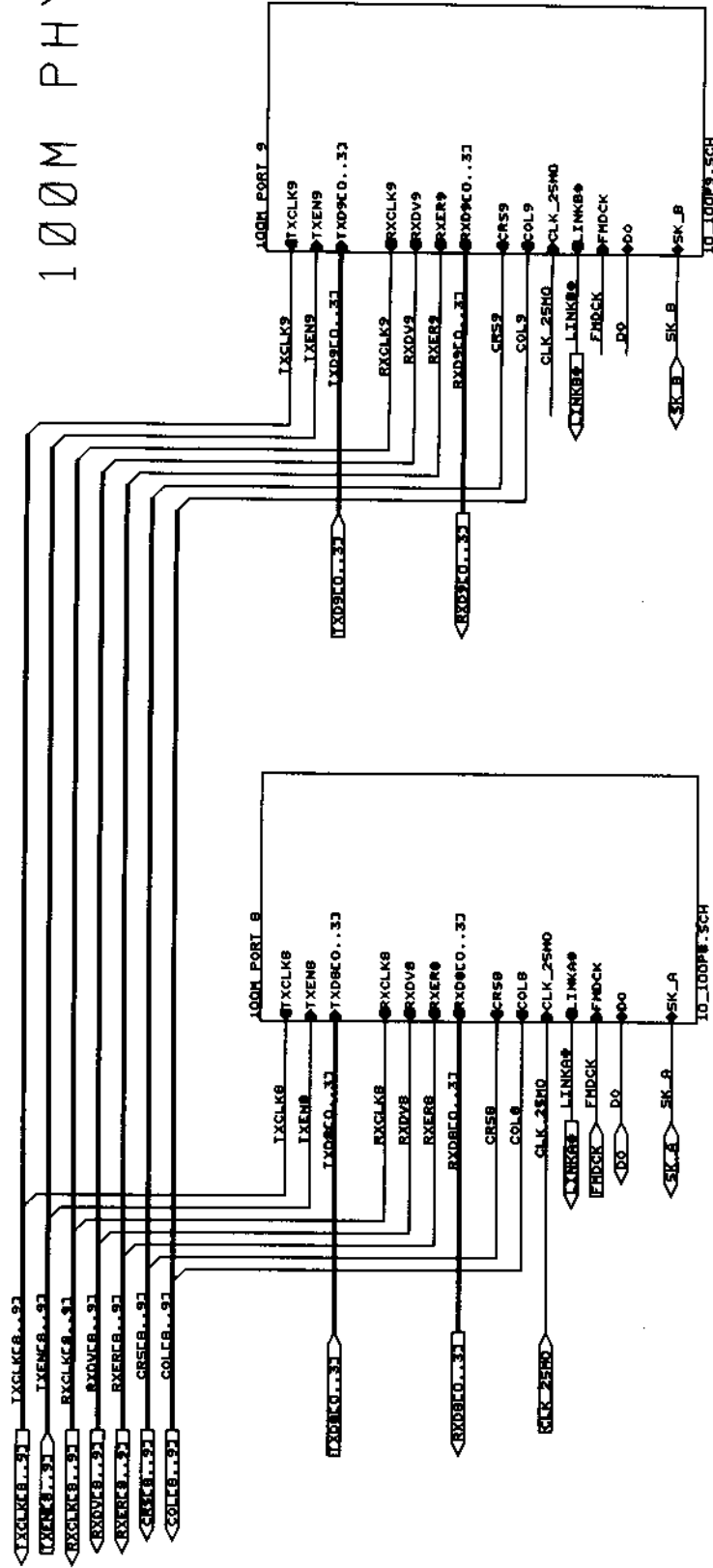
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GT48002



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Date: <b>1998-08-11</b>		Drawn By: <b>POLY PAN</b>	Checked By: <b>POLY PAN</b>
Project: <b>DES810</b>		Sheet: <b>1</b>	Total: <b>1</b>

100M PHY



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 Title: DES-810/DES-818's LON\_FCB

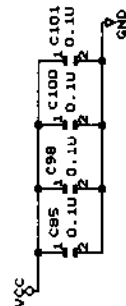
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 Version: A  
 Size Document Number: B  
 Date: March 5, 1997  
 Sheet 14 of 21  
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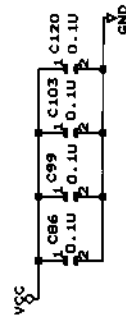
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B:EDIN HIGH;C:USE LOGIC OR MICRO P;
SELLOUT;ECKL;AS 93C4E;5;5K (OUT)
SELLOUT;ECKL;AS 93C4E;5;5K (OUT)
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CHANGE SETTING BY MDC/MDO
CHANGE SETTING BY MDC/MDO

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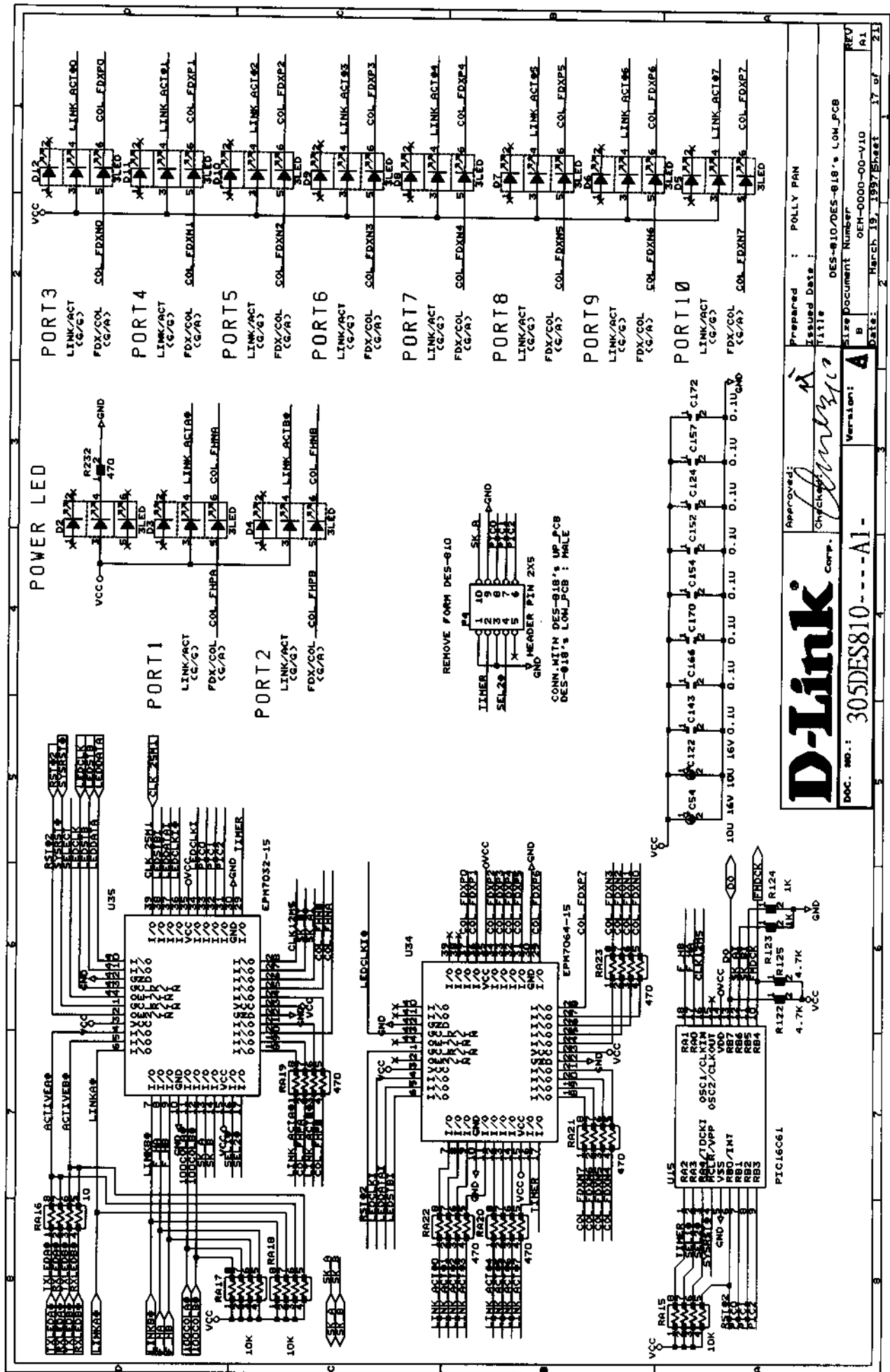
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DOC. NO.: 305DES810-...A1-

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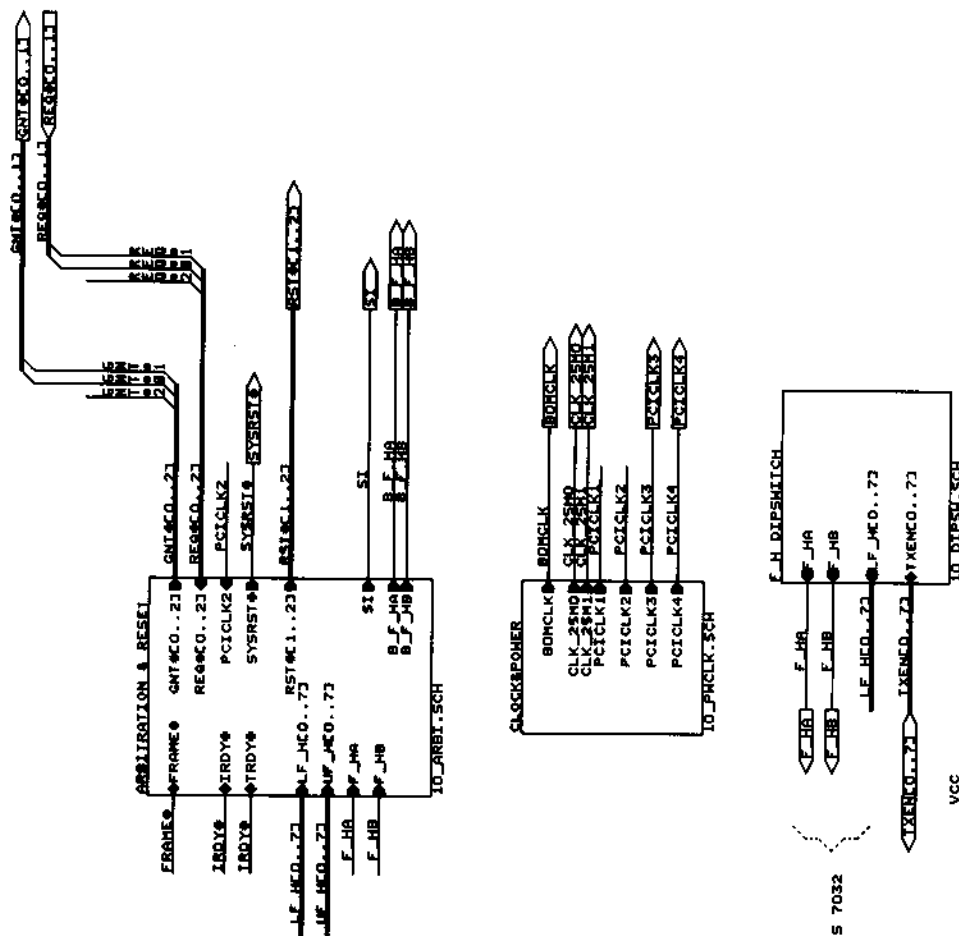
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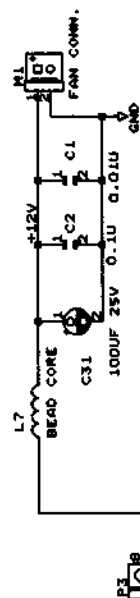
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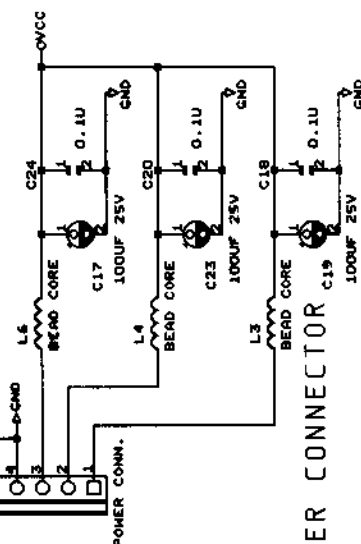
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## FAN CONNECTOR



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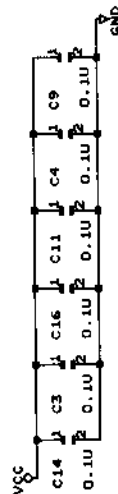
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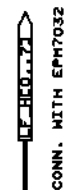
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